APPLICATION NOTE 19

POWER OPERATIONAL AMPLIFIER

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1.0 LOOP STABILITY VS NON-LOOP STABILITY

There are two major categories for stability considerations — Non-Loop Stability and Loop Stability.

Non-Loop Stability covers design areas not related to feedback around the op amp that can cause oscillations in power op amp circuits such as layout, power supply bypassing, and proper grounding.

Loop Stability is concerned with using negative feedback around the amplifier and ensuring that the voltage fed back to the amplifier is less than an additional –180 phase shifted from the input voltage.

The two key factors to troubleshooting an oscillation problem are:

1) What is the frequency of oscillation? (refer to Figure 1 for definitions of UGBW (Unity Gain Bandwidth) and CLBW (Closed Loop Bandwidth) to be used throughout this text)
2) When does the oscillation occur?

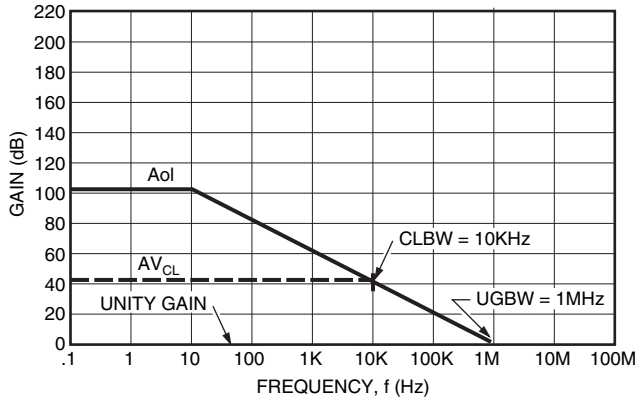


FIGURE 1. DEFINITION OF CLBW & UGBW

The answers to these two questions, along with the sections that follow, should enable you to identify and solve most power op amp stability problems. More importantly, by applying the recommendations in the following sections, you can design power op amp circuits free of oscillation.

2.0 NON-LOOP STABILITY

2.1 CASE GROUNDING

* fosc < UGBW
* oscillates unloaded?—may or may not
* oscillates with V_{IN} = 0?—may or may not

Ungrounded cases of power op amps can cause oscillations, especially with faster amplifiers. The cases of all APEX amplifiers are electrically isolated to allow for mounting flexibility. Because the case is in close proximity to all the internal nodes of the amplifier, it can act as an antenna. Providing a connection from case to ground forms a Faraday shield around the power op amp's internal circuitry that prevents noise pickup and cross coupling or positive feedback.

2.2 RB+ BIAS RESISTOR

* fosc < UGBW
* oscillates unloaded?—may or may not
* oscillates with V_{IN} = 0?—may or may not

Figure 2 is a standard inverting op amp circuit which includes an input bias current matching resistor on the noninverting input. The purpose of this resistor is to reduce input offset voltage errors due to bias current drops across the equivalent impedance as seen by the inverting and non-inverting input nodes. RB+ can form a high impedance node on the noninverting input which will act as an antenna receiving unwanted posi-

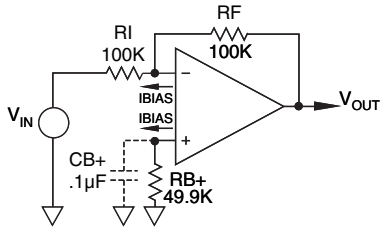


FIGURE 2. RB+

tive feedback. Calculate your DC errors without the resistor. Some op amps have input bias current cancellation negating the effect of RB+. Some op amps have such low input bias currents that the error is insignificant when compared with the initial input offset voltage. Leave RB+ out, grounding the + input, if possible. If the resistor is required, bypass it with a .1 uF capacitor in parallel with RB+ as shown in Figure 2.

2.3 POWER SUPPLY BYPASSING

* fosc < UGBW
* oscillates unloaded?—no
* oscillates with V_{IN} = 0?—may or may not

Supply loops are a common source of oscillation problems. Figure 3 shows a case where the load current flows through the supply source resistance and parasitic wiring or trace resistance. This causes a modulated supply voltage to be seen at the power supply pin of the op amp. This modulated signal is then coupled back into a gain stage of the op amp via the compensation capacitor. The compensation capacitor is usually referred to one of the supply lines as an AC ground.

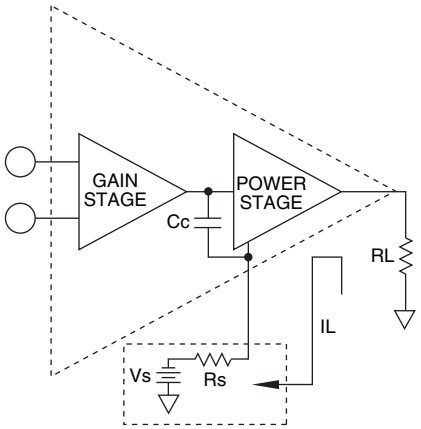


FIGURE 3. IL MODULATION

Figure 4 shows a second case for supply loop oscillation problems. Power supply lead inductance interacts with a capacitive load forming an oscillatory LC, high Q, tank circuit.

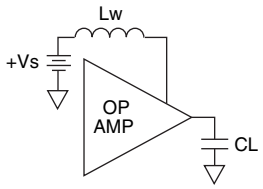
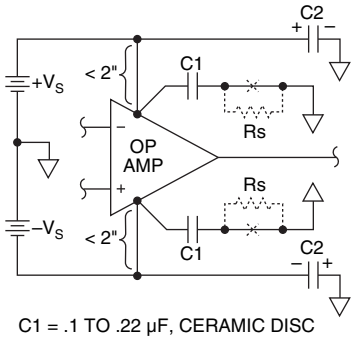


FIGURE 4. LC OSCILLATION

Fortunately, both of the above supply line related problems can be eliminated through the use of proper power supply bypass techniques. Each supply pin must be bypassed to common with a "high frequency bypass" .1uF to .22uF ceramic capacitor. These capacitors must be located directly at the power op amp supply pins. In rare cases where power supply line inductance is high, it may be necessary to add 1 to 10 ohms of resistance in series with the high frequency bypass capacitor to dampen the Q of the resultant LC tank circuit. This additional resistor will probably only be necessary when using a wideband amplifier since amplifiers of 5 MHz unity gain bandwidth or less will not respond to the high frequency oscillation caused by line inductance interacting with the high frequency bypass capacitor. Refer to Figure 5.



C1 = .1 TO .22 µF, CERAMIC DISC
C2 = 10 µF/AMP OUT (PEAK), ELECTROLYTIC
Rs = 3 –10Ω (PROVISIONAL–
HIGHLY INDUCTIVE P.S. LINES)

FIGURE 5. POWER SUPPLY BYPASSING

In addition, a "low frequency bypass" capacitor, minimum value of 10uF per Ampere of peak output current, should be added in parallel with the high frequency bypass capacitors from each supply rail to common. Tantalum capacitors should be used when possible due to their low leakage, low ESR and good thermal characteristics. Aluminum Electrolytic capacitors are acceptable for operating temperatures above 0°C. These capacitors should be located within 2" of the power op amp supply pins. Refer to Figure 5.

2.4 MULTIPLE AMPLIFIER BOARDS

* fosc < UGBW
* oscillates unloaded?—no
* oscillates with V_{IN} =0?—yes

A prototype circuit is built and bench tested to confirm desired performance. Several channels of the same circuit are used on a printed circuit board layout. Much to the dismay of the design engineer, the amplifier circuits on the printed circuit board oscillate. Cross coupling through the power supply lines can be a major problem on multiple amplifier printed circuit boards. Ground the case of each amplifier and ensure each amplifier has its own power supply bypassing per Section 2.3.

2.5 OUTPUT STAGE OSCILLATIONS / OUTPUT R-C SNUBBER

* fosc > UGBW
* oscillates unloaded?—no
* oscillates with V_{IN} = 0?— no, only oscillates over a portion of the output cycle

Sometimes output stages of power op amps can contain local feedback loops that give rise to oscillations. The first type of output stage instability problem arises from a tendency of emitter followers to appear inductive when looking back into their emitter. This occurs if they are driven from a low impedance source and can create output stage oscillations if capacitance is present on the amplifier's output. Refer to Figure 6. This type of instability is rare and usually only shows up when driving load capacitances within a limited range of values.

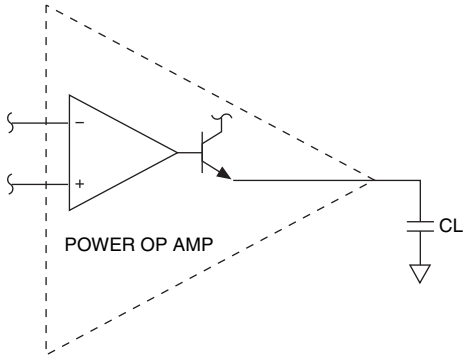


FIGURE 6. EMITTER FOLLOWER WITH C LOAD

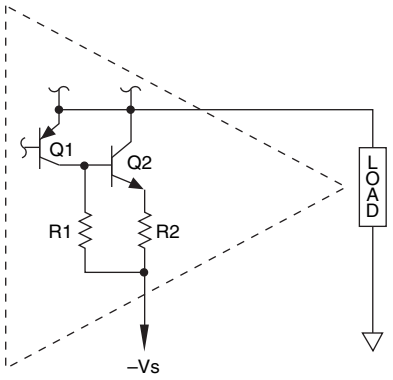


FIGURE 7. COMPOSITE OUTPUT STAGE

The second, more common type of output stage oscillation is due to non-emitter follower output type stages. These stages have heavy local feedback paths. Refer to Figure 7 which is an example of a composite PNP type output stage. This stage is typical of monolithic power op amps where high current PNP

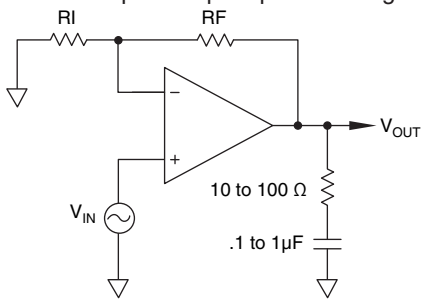


FIGURE 8. OUTPUT R–C SNUBBER

transistors are not readily available. The local feedback in the Q1, Q2 loop will cause output stage oscillations when the output swings negative under reactive loading.

Both of these output stage problems can be fixed by using an R-C Snubber on the output of the op amp to ground or the negative supply rail. This is provided the negative supply rail is properly bypassed per Section 2.3. The Snubber network consists of a 10 to 100 ohm resistor in series with a capacitor of .1 to 1 µF (refer to Figure 8). This network lowers the high frequency gain of the output stage preventing unwanted high frequency oscillations.

2.6 GROUND LOOPS

* fosc < UGBW
* oscillates unloaded?—no
* oscillates with V_{IN} = 0?—yes

Ground loops come about from load current flowing through parasitic layout resistances and wiring. If the phase of the output signal is in phase with the signal at the node it is fed back to, it will result in positive feedback and oscillation. Although these parasitic resistances (RR in Figure 9) in the load current return line cannot be eliminated, they can be made to appear as a common mode signal to the amplifier. This is done by the use of a "star ground" approach. Refer to Figure 9. The star ground is a point that all grounds are referenced to. It is a common point for load ground, amplifier ground, signal ground and power supply ground.

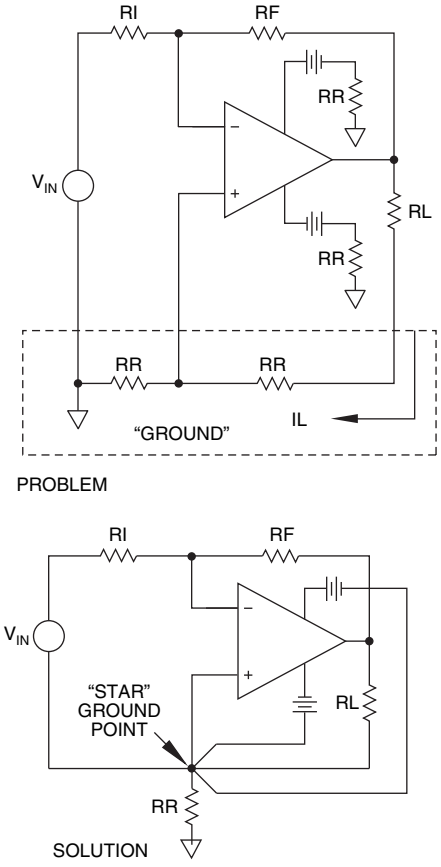


FIGURE 9. GROUND LOOPS

2.7 PRINTED CIRCUIT BOARD LAYOUT

* fosc < UGBW
* oscillates unloaded?—may or may not
* oscillates with V_{IN} = 0?—no

High current output traces routed near input traces can cause oscillations. This is especially true when the output is adjacent to the positive input, giving undesirable positive feedback through capacitive coupling between the adjacent traces. Feedback, input, and bypass components, along with current limit sense resistors, should be located in close proximity to the amplifier.

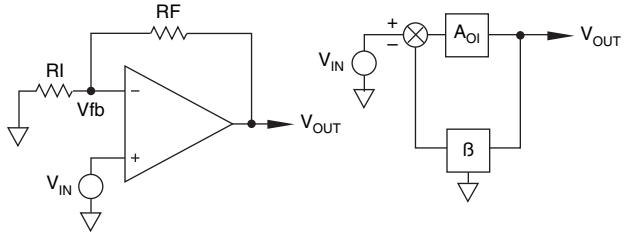
If a printed circuit board has both a high current output trace and a return trace for that high current, then these traces should be routed adjacent to each other (on top of each other on a multi-layer printed circuit board) so they form a twisted pair type of layout. This will help cancel EMI generated outside from feeding back into the amplifier circuit.

3.0 LOOP STABILITY

3.1 BETA SS - FEEDBACK FACTOR

Control theory is applicable to closing the loop around a power op amp. The block diagram in Figure 10 consists of a circle with an X, which represents a voltage differencing circuit. The rectangle with Aol represents the amplifier open loop gain. The rectangle with the ß represents the feedback network. The value of ß is defined as the fraction of the output voltage that is fed back to the input; therefore, ß can range from 0 (no feedback) to 1 (100% feedback).

The term Aol ß that appears in the V_{OUT}/V_{IN} equation in Figure 10, has been called "loop gain" because this can be thought of as a signal propagating around the loop that consists of the Aol and ß networks. If Aol ß is large, there is a lot of feedback. If Aol ß is small, there is not much feedback.



$$Vfb = \frac{V_{OUT}\ RI}{RI + RF}$$

$$Vfb = ß\ V_{OUT}$$

$$ß = \frac{RI}{RI + RF}$$

$$V_{OUT} = V_{IN}\ Aol - Aol\ ß\ V_{OUT}$$

$$\frac{V_{OUT} + Aol\ ß\ V_{OUT}}{V_{IN}} = Aol$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{Aol}{1 + Aol\ ß} = \frac{1}{ß}$$

(FOR: Aol b >> 1)

FIGURE 10. BETA (ß) – FEEDBACK FACTOR

3.2 RATE OF CLOSURE & STABILITY

Refer to Figure 11. Aol is the amplifier's open loop gain curve. 1/ß is the closed loop AC small signal gain in which the amplifier is operating. The difference between the Aol curve and the 1/ß curve is the "loop gain". Loop gain is the amount of signal available to be used as feedback to reduce errors and non-linearities.

A first order check for stability is to ensure when loop gain goes to zero, open loop phase shift must be less than 180 degrees where the 1/ß curve intersects the Aol curve. Another way of viewing that same criteria is to say at the intersection of the 1/ß curve and the Aol curve the difference in the slopes of the two curves, or the RATE OF CLOSURE, is less than or equal to 20 dB per decade. This is a powerful first check for stability. It is, however, not a complete check. For a complete check we will need to check the open loop phase shift of the amplifier throughout its loop gain bandwidth.

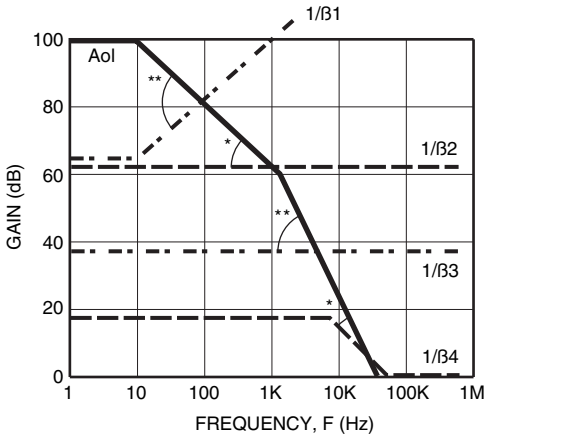


FIGURE 11. RATE OF CLOSURE & STABILITY

A 40 dB per decade RATE OF CLOSURE indicates marginal stability with a high probability of destructive oscillations in your circuit. Figure 11 contains several examples of both stable (20 dB per decade) and marginally stable (40 dB per decade) rates of closure.

3.3 EXTERNAL PHASE COMPENSATION

External phase compensation is often available on an op amp as a method of tailoring the op amp's performance for a given application. The lower the value of compensation capacitor used the higher the slew rate of the op amp. This is due to fixed current sources inside the front end stages of the op amp. Since current is fixed, we see from the relationship of I = CdV/dt that a lower value of capacitance will yield a faster voltage slew rate.

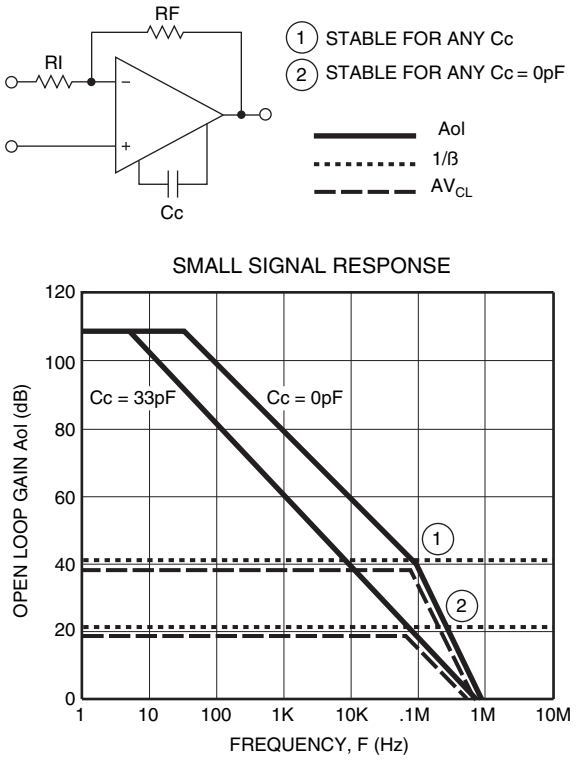


FIGURE 12. EXTERNAL PHASE COMPENSATION

However, the advantage of a faster slew rate has to be weighed against AC small signal stability. In Figure 12 we see the Aol curve for an op amp with external phase compensation. If we use no compensation capacitor, the Aol curve changes from a single pole response with Cc = 33pF, to a two pole response with Cc = 0pF. Curve 1 illustrates that for 1/ß of 40 dB the op amp is stable for any value of external compensation capacitor (20 dB/decade rate of closure for either Aol curve, Cc = 33pF or Cc = 0pF). Notice that 1/ß curve continues on past the intersection of the Aol curve. At the intersection of 1/ß and Aol, the AV_{CL} closed loop gain curve, or V_{OUT}/V_{IN} gain begins to roll off and follow the Aol curve. This is because there is no loop gain left to keep the closed loop gain flat at higher frequencies.

Curve 2 illustrates that for 1/ß of 20 dB and Cc = 0pF, there is a 40 dB/decade rate of closure or marginal stability. To have stability with Cc = 0pF minimum gain must be set at 40dB. This requires a designer to not only look at slew rate advantages of decompensating the op amp, but also at the gain necessary for stability and the resultant small signal bandwidth.

3.4 STABILITY - RATE OF CLOSURE

Figure 13 shows a typical single pole op amp configuration in the inverting gain configuration. Notice the additional V_{NOISE} voltage source shown at the +input of the op amp. This is shown to aid in conceptually viewing the 1/ß plot.

An inverting amplifier with its +input grounded, will always have potential for a noise source to be present on the +input . Therefore, when one computes the 1/ß plot, the amplifier will appear to run in a gain of 1 + RF/RI for small signal AC. The V_{OUT}/V_{IN} relationship will still be –RF/RI. This is also why an amplifier can never run at a gain of less than one for small signal AC stability considerations.

The plot in Figure 13 shows the open loop poles from the amplifier's Aol curve, as well as the poles and zeroes from

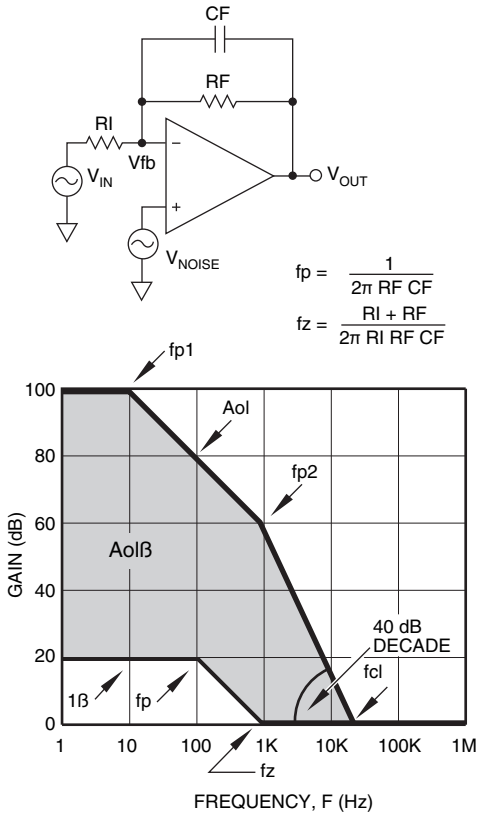


FIGURE 13. STABILITY– RATE OF CLOSURE

the 1/ß curve. The locations of fp and fz are important to note as we will see that poles in the 1/ß plot will become zeroes and zeroes in the 1/ß plot will become poles in the open loop stability check.

Notice that at fcl the RATE OF CLOSURE is 40 dB per decade indicating a marginal stability condition. The difference between the Aol curve and 1/ß curve is labelled Aol ß which is also known as loop gain.

3.5 STABILITY - OPEN LOOP

Stability checks are easily performed by breaking the feedback path around the amplifier and plotting the open loop magnitude and phase response. Refer to Figure 14. This open loop stability check has the first order criteria that the slope of the magnitude plot as it crosses 0 dB must be 20 dB per decade for guaranteed stability.

The 20 dB per decade is to ensure the open loop phase does not dip to –180 degrees before the amplifier circuit runs out of loop gain. If the phase did reach -180, the output voltage would now be fed back in phase with the input voltage (-180 degrees phase shift from negative feedback plus -180 degrees phase shift from feedback network components would yield -360 degrees phase shift). This condition would continue to feed upon itself causing the amplifier circuit to break into uncontrollable oscillations.

Notice in Figure 14 this open loop plot is really a plot of Aol ß. The slope of the open loop curve at fcl is 40 dB per decade indicating a marginally stable circuit. As shown, the zero from the 1/ß plot in Figure 13 became a pole in the open loop plot in Figure 14 and likewise the pole from the 1/ß plot in Figure 13 became a zero in the open loop plot of Figure 14. We will use this knowledge to plot the open loop phase plot to check for stability. This plot of the open loop phase will provide a complete stability check for the amplifier circuit. All the information we need will be available from the 1/ß curve and the Aol curve.

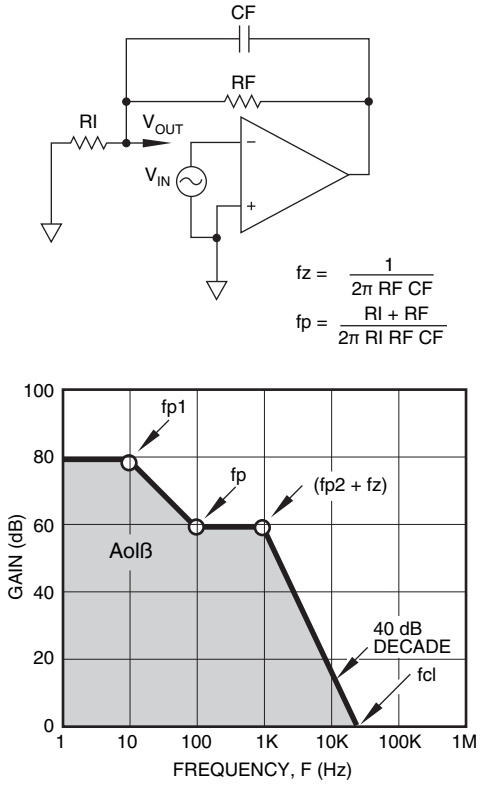
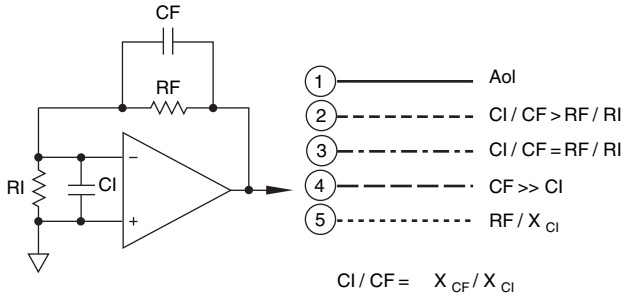


FIGURE 14. STABILITY– OPEN LOOP

4.0 STABILITY & THE INPUT POLE / INPUT & FEEDBACK IMPEDANCE

* fosc < CLBW
* oscillates unloaded?—yes
* oscillates with V_{IN} = 0?—yes

All op amps have some input capacitance, typically 6-10 pF. Printed circuit layout and component leads can introduce additional input stray capacitances. When high values of feedback and input resistors are used, this input capacitance will contribute an additional pole to the loop gain response (a zero in the 1/ß plot, a pole in the open loop phase check for stability, or a pole in the Aol ß, loop gain, plot).



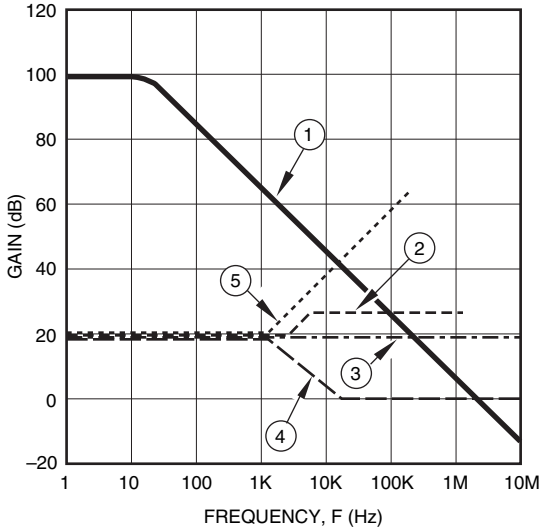


FIGURE 15. THE INPUT POLE

We will refer to Figure 15 for a detailed look at the input pole and stability. Remember, our first order criteria for stability is a Rate Of Closure of 20dB per decade or less. Curve 1 is the op amp's Aol plot. Curve 5 shows the effect of input capacitance with no CF feedback capacitor. We see the rate of closure is 40 dB per decade and marginal stability exists. With just CI present, as frequency increases, the impedance from the -input of the op amp decreases, thereby causing the 1/ß plot to increase (remember X_{CI} = 1/2πfCI). If we now add some small value of CF as in Curve 2 we see the 1/ß plot flatten out to intersect the Aol at a rate of closure 20 dB per decade implying stability. If we further increase CF, as in Curve 3, such that both breakpoints are the same frequency, we will have ZF/ZI constant over frequency and the 1/ß plot will be flat with frequency. This yields the ever-stable 20 dB per decade rate of closure. If we then continue to increase CF as in Curve 4, we will see CFdominate as frequency increases and the net result is a low pass filter frequency roll-off. For this case the op amp must be unity gain stable, since the op amp operates at a gain of one for frequencies above 10KHz.

Often you will see CF recommended to be used to decrease overshoot and improve settling time for a transient input into a given op amp circuit. In the AC small signal domain, we are merely optimizing the circuit for stability.

Minimize values of feedback and input resistor values. This will reduce the effect of the input pole as well as help reduce DC errors by keeping voltage drops due to bias currents low. A summing node of an op amp can pick up unwanted AC signals and amplify them if that node is high impedance. Keeping the feedback and input resistance values low will reduce the impedance at the summing nodes and minimize stray signal pick up. Practical values for feedback and input resistance values are from 100 ohms to 1 megaohm.

5.0 LOOP STABILITY EXAMPLES

5.1 VOLTAGE TO CURRENT CONVERSION— FLOATING LOAD

* fosc < CLBW
* oscillates unloaded ? — yes
* oscillates with V_{IN} = 0 ? — yes

Figure 16 illustrates a common voltage to current conversion circuit. The input command voltage of +/-10V is scaled to control -/+1.67A of output current through the load.

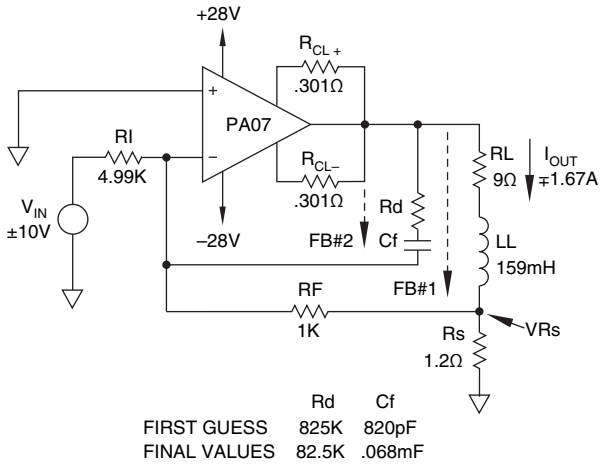


FIGURE 16. V-I CIRCUIT AND STABILITY

This V-I (Voltage to Current) topology is a floating load drive. Neither end of the load, series RL and LL, is connected to ground.

The easiest way to view the voltage feedback for load current control in this circuit is to look at the point of feedback which is the top of Rs. The voltage gain VRs/Vin is simply -RF/RI which translates to (–1K/4.99K = -.2004). The Iout/Vin relationship is then VRs/Rs or Iout = - Vin (RF/RI)/Rs which for this circuit is (Iout = -.167 Vin). We will use our knowledge of 1/ß, Rate of Closure, and open loop stability phase plots, to design this V-I circuit for stable operation. There are two voltage feedback paths around the amplifier, FB#1 and FB#2. We will analyze FB#1 first and then see why FB#2 is necessary for guaranteed stability.

STABILITY SOLUTION FOR V-I CIRCUIT

STEP 1: On Figure 17 plot the op amp's Aol curve as given by the manufacturer.

STEP 2: On Figure 17 plot FB#1. Refer to Figure 18 for calculation of FB#1. At DC, LL is a short and so ß is a voltage divider through resistors as shown in Figure 18. As we go to higher frequencies, the reactance of LL will increase (XL = 2πfL). This will increase the net load impedance

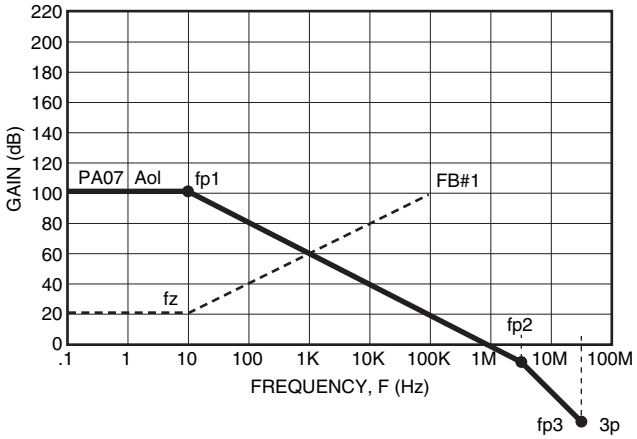


FIGURE 17. Aol AND FB # 1 – MAGNITUDE PLOT FOR STABILITY

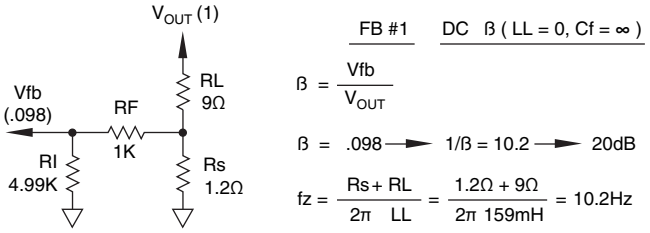


FIGURE 18. FEEDBACK NO.1 (FB #1)

which will cause ß to decrease and 1/ß to increase as frequency increases. Since we are working with a single reactive element the increase of that gain will be 20 dB per decade. Figure 18 details the breakpoint fz where this increase begins. We see that at the intersection of FB#1 and the PA07 Aol curves the rate of closure is 40 dB per decade indicating marginal stability.

STEP 3: Refer to Figure 19 which repeats PA07 Aol and FB#1. We will add FB #2 to force the high frequency part of the 1/ß curve to flatten out and intersect the PA07 Aol curve at 20 dB per decade. FB #2 will dominate at frequencies above 1 KHz. Although our V-I circuit has two feedback paths, the op amp will follow whichever feedback path is dominant. This means the larger ß is, the more voltage is fed back from the output to the -input as negative feedback (Remember ß = Vfb/V_{OUT}). With a larger ß, 1/ß will become smaller; therefore, the dominant feedback path out of FB#1 and FB#2 will be the lowest gain path.

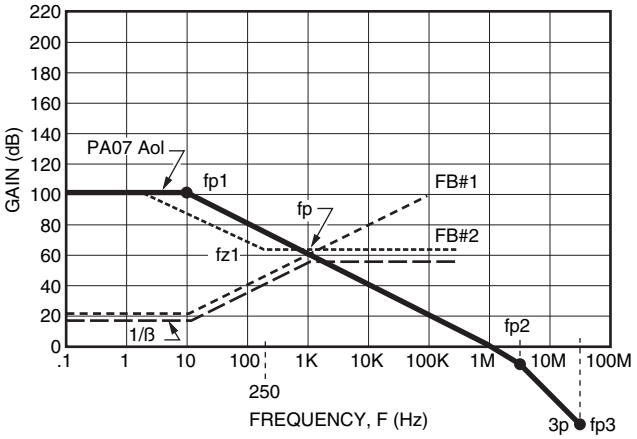


FIGURE 19. FIRST GUESS MAGNITUDE PLOT FOR STABILITY

Plot a desired feedback path for FB#2. At high frequencies, FB#2 will be a flat line since Cf will be a short leaving a pure resistive divider for ß. At DC, FB#2 will be infinite since Cf is an open. This will be limited by the PA07 Aol curve. Since we only have one reactive element in FB#2, we will have a 20 dB per decade slope from low to high frequency. Set fz1 one half to one decade below the intersection of FB#1 and FB#2. This "Decade" rule of thumb ensures that as component values and Aol curves vary we will not get into stability trouble—more about this later.

STEP 4: In Figure 19 the long-dashed line represents the 1/ß feedback path that the PA07 operates in for small signal AC. According to our first order check for stability we see a 20 dB per decade rate of closure indicating a stable design. But let's do our complete stability check by using the 1/ß curve and PA07 Aol curve to plot the open loop phase plot. Remember the following rules when plotting open loop phase plots for stability checks.

RULES FOR PLOTTING OPEN LOOP PHASE PLOTS

1) Poles in 1/ß plot become zeroes in the open loop stability check.
2) Zeroes in 1/ß plot become poles in the open loop stability check.
3) Poles and zeroes in the Aol curve of the op amp remain respectively poles and zeroes in the open loop stability check since the op amp Aol curve is an open loop curve already.
4) Phase for poles is represented by a -45 degree phase shift at the frequency of the pole with a -45 degree per decade slope, extending this line with 0 degree and -90 degree horizontal lines.
5) Phase for zeroes is represented by a +45 degree phase shift at the frequency of the zero with a +45 degree per decade slope, extending this line with 0 degree and +90 degree horizontal lines.

Figure 20 is the resultant open loop phase plot using the information from Figure 19. After plotting individual open loop poles and zeroes, and drawing the appropriate slopes, we graphically add the slopes to yield a resultant open loop phase as shown in Figure 20. Notice fp3 in Figure 20 is a triple pole. It is easier to plot this as shown in Figure 20 as three poles "on top" of each other. This makes it easier to add graphically for a resultant open loop phase plot. As shown in Figure 20, our open loop phase dips to -180 at 100Hz. Our first attempt at compensation was not successful since we desire at least 45 degrees of phase margin (open loop phase should not dip to less than -135 degrees).

STEP 5: We need to revisit FB#2 to make this V-I circuit stable. Figure 21 shows a new FB#2 and the resultant 1/ß plot. Before we look at the open loop phase plot, let's discuss Figure 21. We see that in the PA07 Aol curve there is a pole at fp1, 10Hz, which will be a pole in our open loop phase plot. We also see a zero at fz, 10Hz, in the 1/ß plot, which will become a pole in our open loop phase plot. Now we have two poles at 10Hz in our open loop

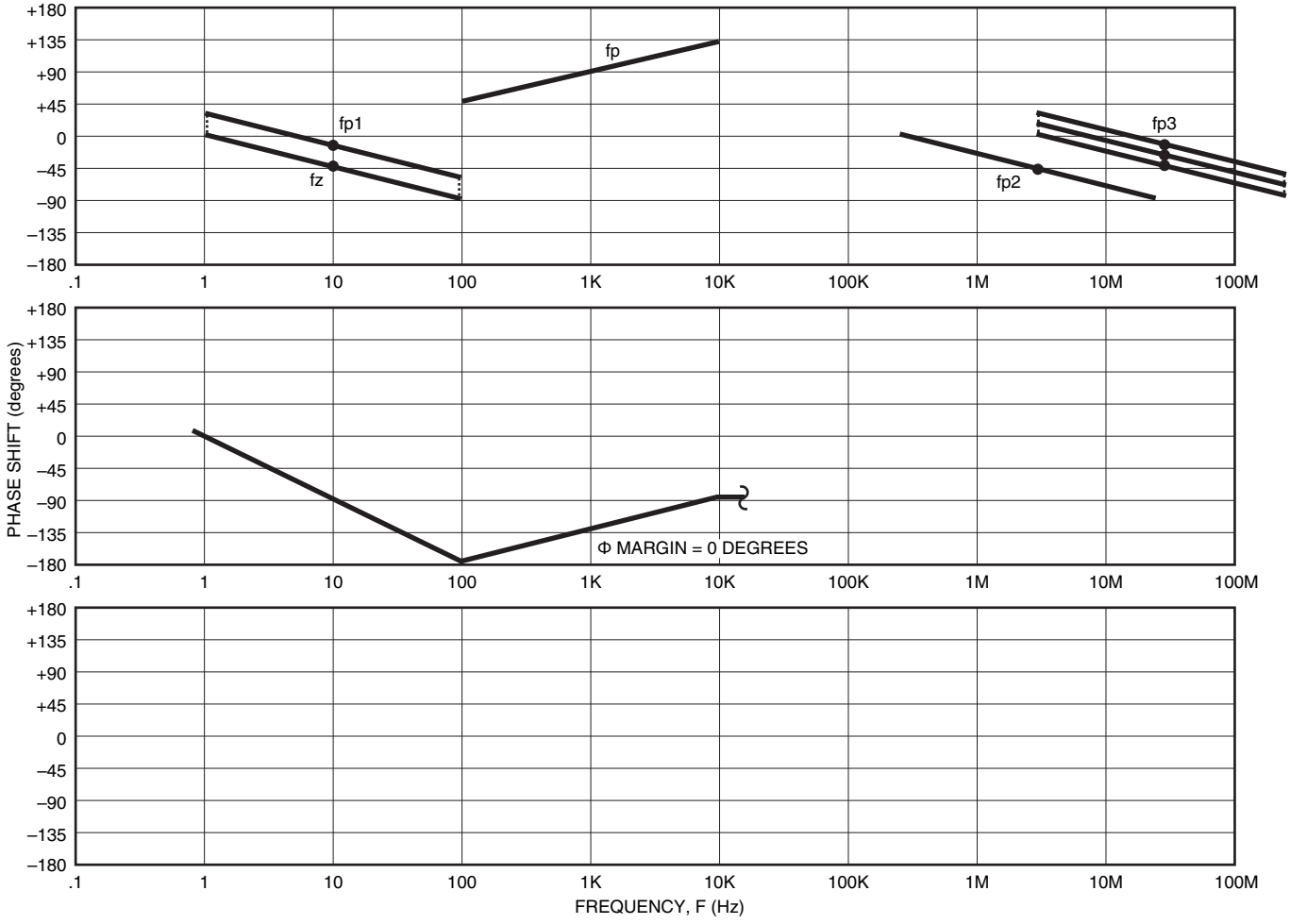


FIGURE 20. FIRST GUESS OPEN LOOP PHASE PLOT FOR STABILITY

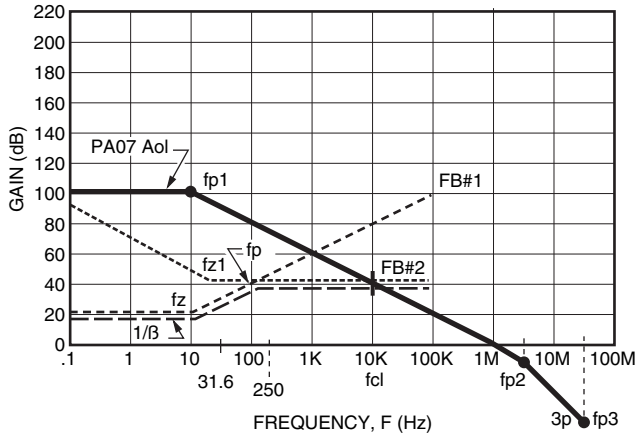


FIGURE 21. FINAL VALUE MAGNITUDE PLOT FOR STABILITY

phase plot. To keep the open loop phase from reaching -180, we must add a zero at 100Hz to get 45 degrees of phase margin. Poles and zeroes a decade beyond fcl, the intersection of 1/ß and PA07 Aol, are of no concern for stability since at fcl the loop gain is zero. The reason we must look a decade beyond fcl on the magnitude plot is that poles and zeroes have an effect on phase plus or minus a decade away from their physical location on the magnitude plot.

Viewing the magnitude plot in this way can help us save iterative steps in compensating to guarantee good stability. Refer to Figure 22 for final open loop phase plot stability.

Once the open loop phase plot verifies stability, it is time to compute final values for FB#2 components Rd and Cf. Figure 23 (next page) details these calculations. Notice in Figure 23 that to work with ß it is easiest to set Vout to 1 which then allows us to easily use voltage dividers and currents to calculate values for Rd. Cf is computed as given by the formula in Figure 23.

OPEN LOOP PHASE PLOTS FOR STABILITY — FINAL NOTE:

This hand plotting technique is a linear graphical method. Actual magnitude plots run on such analog circuit simulations as SPICE will be 3 dB different and actual phase plots will be 6 degrees different.

5.2 CAPACITIVE LOADING & STABILITY

* fosc < CLBW
* oscillates unloaded?—no
* oscillates with V_{IN} = 0?—yes

5.2.1 CAPACITIVE LOADING - GENERAL

Refer to Figure 24 (next page) for discussion of power op amps and capacitive loading. The output impedance of a power op amp, Ro, can interact with capacitive loads and form an additional high frequency pole in the op amp's Aol curve. This modified Aol curve is what we must look at for stability checks. In Figure 24, we see a modified Aol curve whose slope changes from 20 dB per decade to 40 dB per decade at 10 kHz. Note that the rate of closure for this circuit is 40 dB per decade indicating marginal stability.

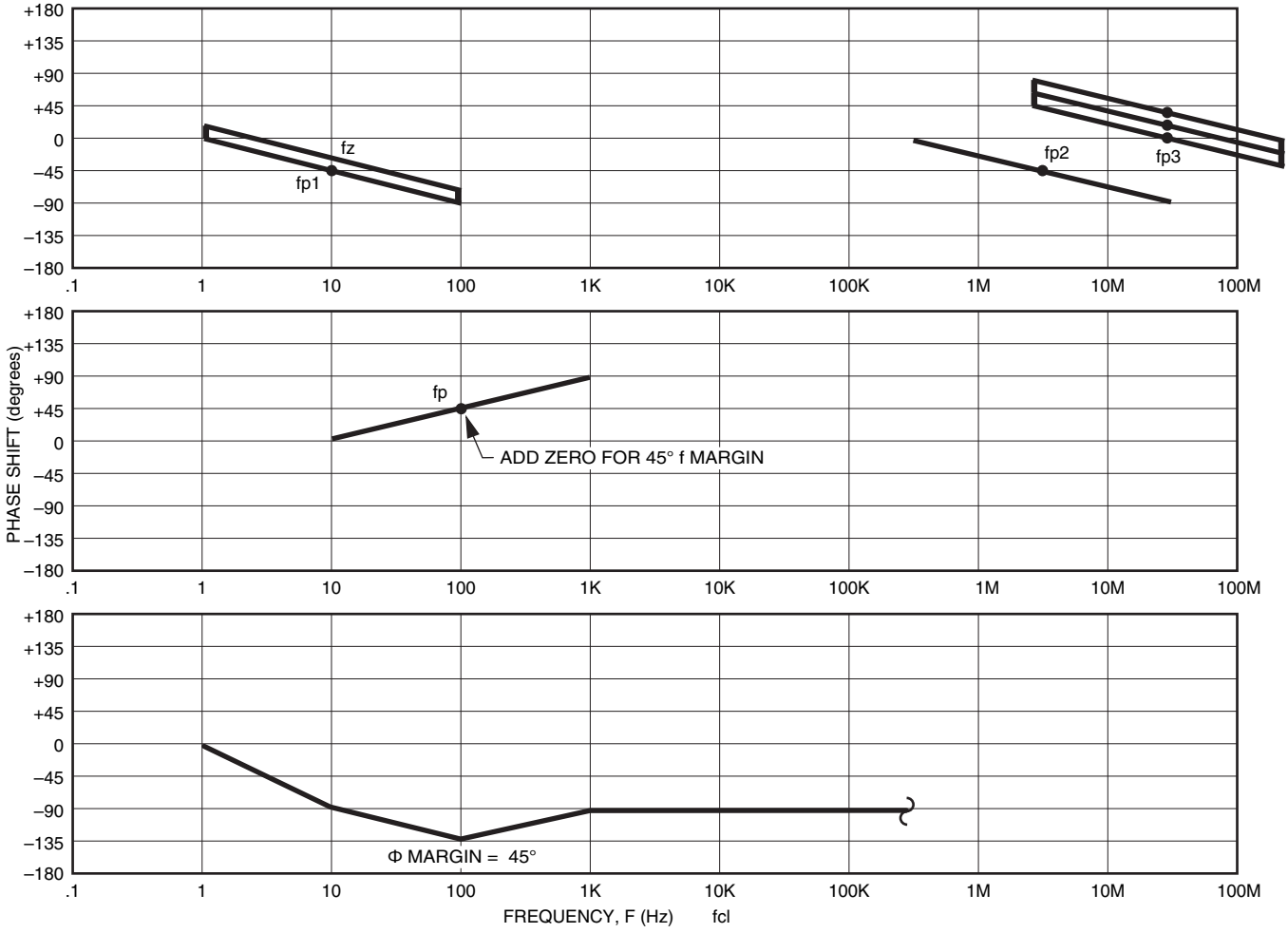


FIGURE 22. FINAL VALUE OPEN LOOP PHASE PLOT FOR STABILITY

5.2.2 CABLE AND CAPACITIVE LOADING

Beware of coaxial cables which can appear capacitive. A coaxial cable appears capacitive, instead of its characteristic impedance, resistive, if the length of the cable is less than one-fortieth of the wavelength in the cable at the frequency of interest, f. This length, l, is given by:

$$l \leq \frac{1}{40} \frac{Kc}{f} \text{ meters}$$

where K is a propagation constant that is sometimes called the velocity factor (0.66 for coaxial cable) and c is the velocity of light (3.00 X10^8 m/s).

EXAMPLE: If f = 10KHz:

$$l \leq \frac{1}{40} \frac{(0.66)\ (3x10^8)}{10^4} = 495 \text{ meters (1624 feet)}$$

Cables less than 495 meters will appear capacitive for 10 kHz signals at the rate of 95 pF/meter (29 pF/foot) for RG-58A/U, a commonly used coaxial cable.

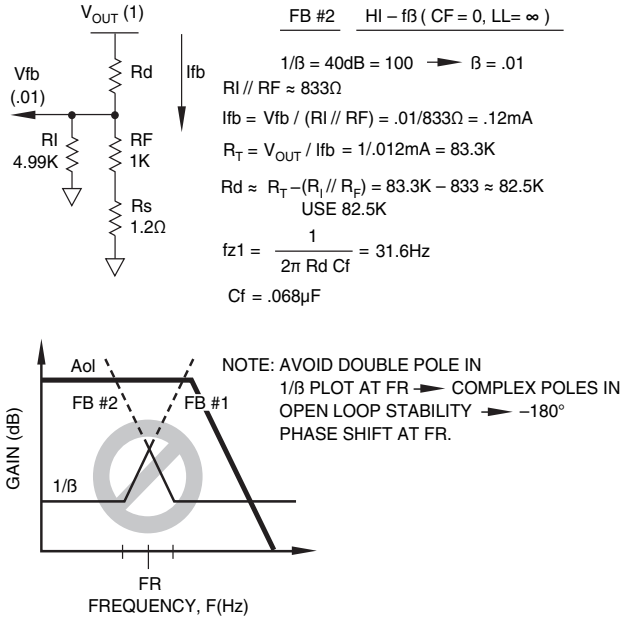


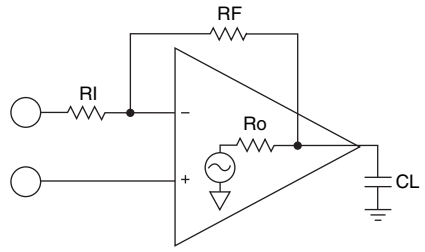
FIGURE 23. FEEDBACK NO. 2 (FB #2) FINAL VALUE CALCULATIONS

5.2.3 AMPLIFIER OUTPUT IMPEDANCE, RO AND CAPACITIVE LOADING

In the design of power amp circuits, the need often arises for a power amp model with specified output impedance. Most often, this requirement revolves around the need to accurately predict the phase performance of power amp circuits.

Output impedance of any op amp is modified by the feedback network present around the device. In voltage source type circuits, the effect of the network is to reduce the output impedance by a factor equal to the ratio of open loop gain to closed loop gain. In power amps, the net result is an effective output impedance of milliohm levels at frequencies below 1kHz. Wiring and interconnections often create larger impedances than the output impedance of the closed loop power amp. Therefore, output impedance will play a minor role in the phase performance at low frequencies. At high frequencies, reactive load considerations are already addressed by capacitive load specifications given on many power amplifiers.

Within the bandwidth of the amplifier the output impedance of most APEX power op amps appears predominantly resistive. As an output stage drives higher currents, its output impedance



UNITY GAIN STABLE AMPLIFIER
BUT: UNSTABLE 40 dB/DECADE WITH CL

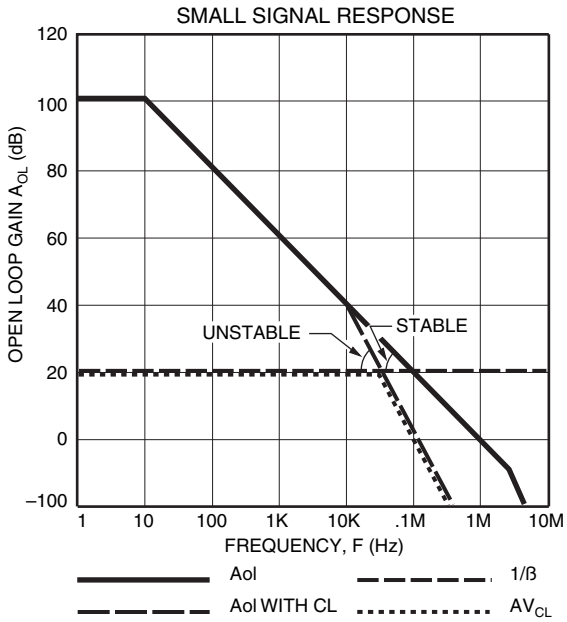


FIGURE 24. CAPACITIVE LOADING

changes when compared to the low current or unloaded output impedance. In general, this impedance reduces as current is driven through the output stage.

When compensating circuits with capacitive loading we will use the low current or unloaded output impedance for Ro. This will be the highest value of Ro causing the lowest frequency additional pole which modifies an amplifier's Aol curve when driving a capacitive load. Many designs in the past have verified that compensating for this condition will give the best stability for all conditions when driving capacitive loads.

The following is a list of output impedances for APEX power op amps and boosters.

OP AMP OR BOOSTER	OUTPUT IMPEDANCE
PA01	2.5-8.0 ohms
PA02	10-15 ohms
PA03	25 ohms
PA04	2.0 ohms
PA05	5 ohms
PA07	1.5-3.0 ohms
PA08	1.5K-1.9K ohms
PA09	15-19 ohms
PA10	2.5-8.0 ohms
PA12	2.5-8.0 ohms
PA19	30-40 ohms
PA51	1.5-1.8 ohms

PA61 . . . . . 1.5-1.8 ohms
PA73 . . . . . 1.5-1.8 ohms
PA81J . . . . . 1.4K-1.8K ohms
PA82J . . . . . 1.4K-1.8K ohms
PA83 . . . . . 1.4K-1.8K ohms
PA84 . . . . . 1.4K-1.8K ohms
PA85 . . . . . 50 ohms
PA88 . . . . . 100 ohms
PA89 . . . . . 100 ohms
PB50 . . . . . 35 ohms
PB58 . . . . . 35 ohms

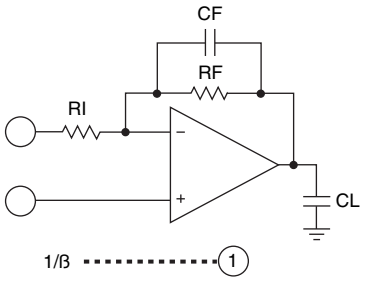
5.2.4 COMPENSATING CAPACITIVE LOADS

There are two main ways to compensate for capacitive loads or two pole Aol curves. The "Feedback Zero" and "Noise Gain" or "Input R-C Network" compensation techniques for capacitive loads will both be discussed.

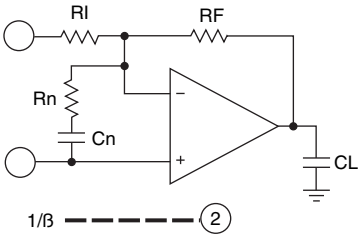
The "Feedback Zero" technique uses a pole in the 1/ß plot (a zero in the open loop phase check for stability or a zero in the Aol ß, loop gain, plot) to compensate for the additional pole due to capacitive loading in the amplifier's modified Aol curve. Refer to Figure 25. Note that in Curve 1 there is both a pole and zero in this 1/ß plot. The pole is due to the interaction of Rf and Cf. The zero can be found by graphically extending the 1/ß plot to zero dB. Remember from previous discussion that an op amp cannot operate at a gain of less than 1 for small signal AC.

The "Noise Gain" compensation technique raises the small signal AC gain of the amplifier to run at a gain that is high enough to ignore the additional high frequency pole in the Aol curve due to capacitive loading. Refer to Figure 25. Curve 2 shows the 1/ß plot for noise gain compensation.

Notice in Figure 25 that both Curve 1 and Curve 2 yield a 20 dB per decade rate of closure implying stability; whereas, with just resistive feedback at the given gains the circuits would be unstable with a 40 dB per decade rate of closure.



FEEDBACK ZERO COMPENSATION



NOISE GAIN COMPENSATION

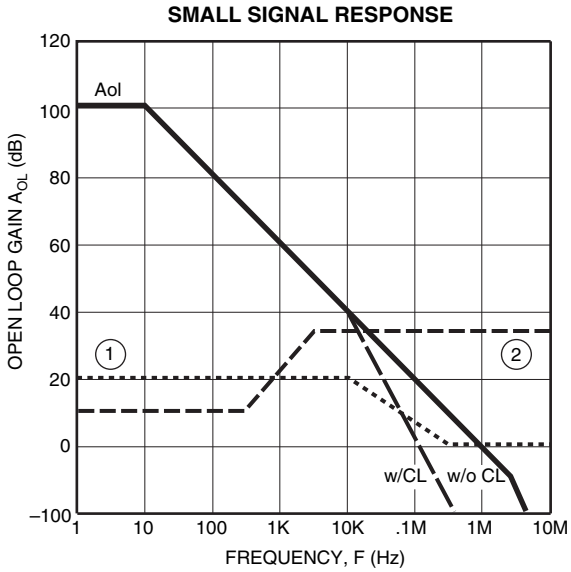


FIGURE 25. CAPACITIVE LOAD COMPENSATION

5.2.4.1 FEEDBACK ZERO COMPENSATION

Figure 26 illustrates a circuit utilizing Feedback Zero Compensation for stability when driving a capacitive load. Figure 27 is our magnitude plot to work with for stability. The following procedure will ensure a logical approach to optimize stability:

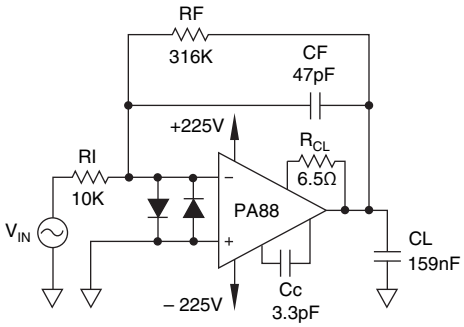


FIGURE 26. FEEDBACK ZERO COMPENSATION FOR CL

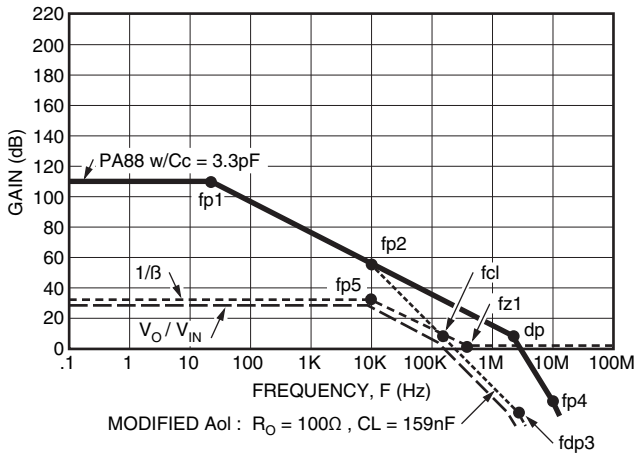


FIGURE 27. FEEDBACK ZERO COMPENSATION FOR CL
MAGNITUDE PLOT FOR STABILITY

STEP 1: Modify the PA88 Aol due to CL. Here we use the output impedance number for the PA88 of Ro = 100 ohms.

$$fp2 = \frac{1}{2\pi\ Ro\ CL} = \frac{1}{2\pi\ 100\ 159nF} = 10\ kHz$$

The higher frequency poles of the unmodified PA88 Aol must be added into the modified Aol as shown in Figure 26.

STEP 2: Calculate DC ß for circuit.

DC ß = RI/(RF + RI) = 10K/(316K+10K) = .030674846

DC 1/ß = 20 Log (1/.030674846) = 30.26 dB

STEP 3: Plot DC 1/ß. Add pole in 1/ß plot to compensate for fp2. Ensure fp5 is one-half to one decade away from fcl such that if the modified Aol plot in the real world moves to the left towards lower frequency we will not be back at a 40 dB per decade rate of closure. Note in Figure 27 that the 1/ß plot has fp5 and fz1. The feedback network continues to feed back output voltage beyond fcl until we reach 0 dB. Then the 1/ß plot flattens out at 0 dB. It is important to include fz1 since it will be a pole in our open loop phase check and will affect phase at frequencies lower than fcl. At fcl loop gain is zero and beyond fcl we are not concerned with phase shift to guarantee stability. Note that the V_O/V_{IN} plot follows the 1/ß plot until at which point there is no loop gain and V_O/V_{IN} will follow the Aol curve on down in gain.

STEP 4: Plot open loop phase as in Figure 28. We see we have 67 degrees of phase margin and therefore guaranteed stability.

STEP 5: Once you have chosen CF to get the fp5 you want you automatically set fz1. fz1 can be gotten graphically from the 1/ß plot. For those of you who want exact breakpoints, here are the formulae for the 1/ß plot in Figure 27.

$$fp5 = \frac{1}{2\pi\ RF\ CF}$$

$$fz1 = \frac{RI + RF}{2\pi\ CF\ RI\ RF}$$

5.2.4.2 NOISE GAIN COMPENSATION

Figure 29 (next page) illustrates how Noise Gain compensation works. One way to view noise gain circuits is to treat the amplifier as a summing amplifier. There are two input signals into this inverting summing amplifier. One is V_{IN} and the other is a noise source summed in via ground through the series combination of Rn and Cn. Since this is a summing amplifier, V_O/V_{IN} will be unaffected if we sum zero into the Rn-Cn network. However, in the small signal AC domain, we will be changing the 1/ß plot of the feedback as when Cn becomes a short and if Rn << RI the gain will be set by RF/Rn. Figure 29 shows the equivalent circuits for AC small signal analysis at low and high frequencies.

Notice in Figure 29 that the V_O/V_{IN} relationship is flat until the Noise Gain forces the loop gain to zero. At that point, fcl, the V_O/V_{IN} curve follows the Aol curve since loop gain is gone to zero. Since noise gain introduces a pole and a zero in the 1/ß plot, here are a few tips to keep phase under control for guaranteed stability. Keep the high frequency flat part of the noise gain no higher in magnitude than 20 dB greater than the low frequency gain. This will force fp and fz in Figure 29 to be no more than a decade apart. This will also keep the phase from dipping to -135 since there is usually an additional low frequency pole due to the amplifier's Aol already contributing an additional -90 degrees in the open loop phase plot. Keep fp one half to one decade below fcl to prevent a rate of closure of 40 dB per decade and prevent instability if the Aol curve shifts

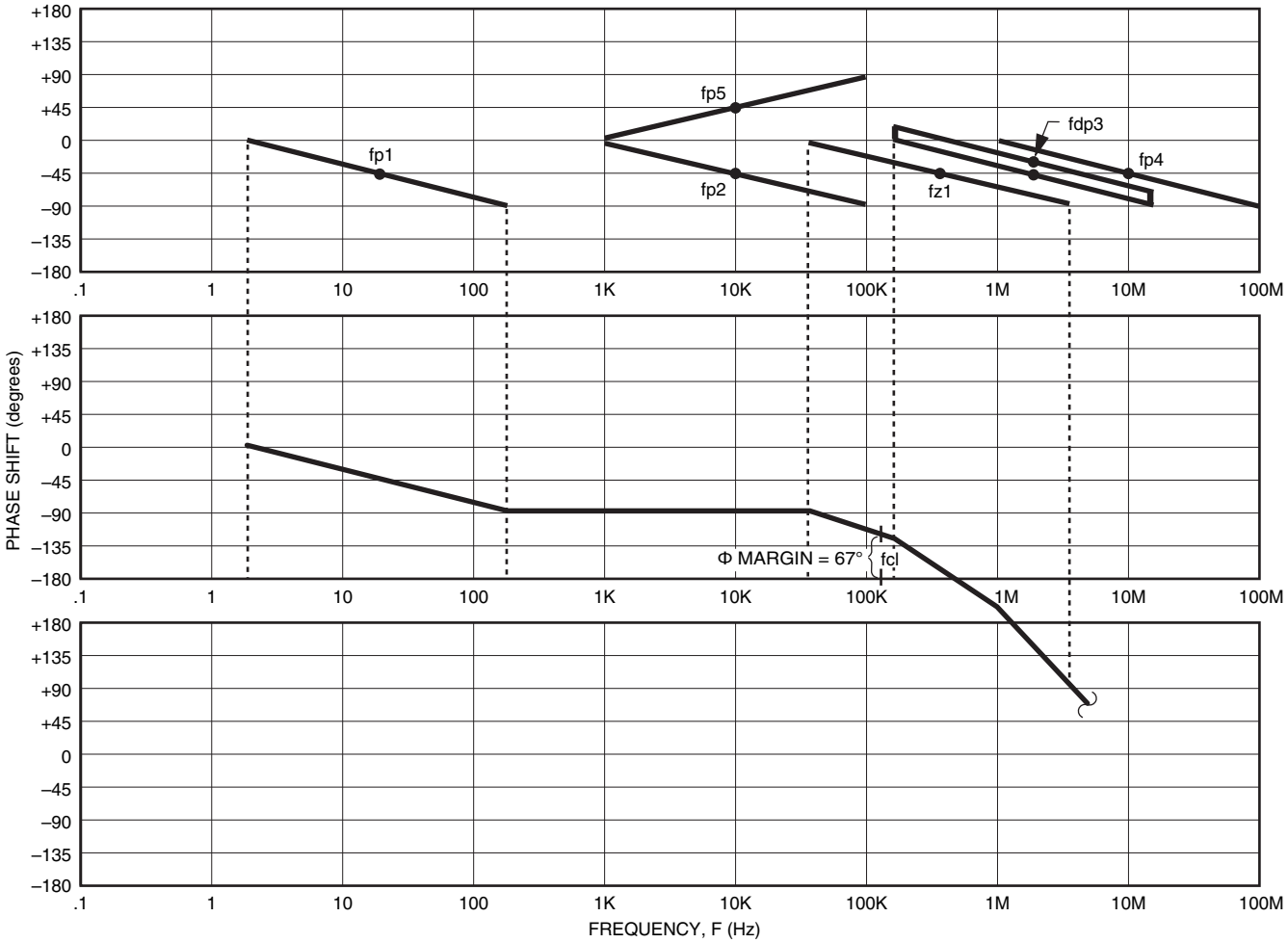


FIGURE 28. FEEDBACK ZERO COMPENSATION FOR CL OPEN LOOP PHASE PLOT FOR STABILITY

to the left which can happen in the real world.

Usually one selects the high frequency gain and sets fp. fz can be gotten graphically from the 1/ß plot. Once again for completeness, here are the formulae for noise gain poles and zeroes:

$$fp = \frac{1}{2\pi\ Rn\ Cn} \qquad fz = \frac{RF + RI}{(2\pi)\ (Cn)\ (RFRI + RFRn + RIRn)}$$

Figure 30 illustrates a circuit utilizing noise gain compensation for stability when driving a capacitive load. Figure 31 is our magnitude plot to work with for stability.

The following procedure will ensure a logical approach to optimize stability:

STEP 1: Modify the PA88 Aol due to CL. Here we use the output impedance number for the PA88 of Ro = 100 ohms.

$$fp2 = \frac{1}{2\pi\ Ro\ CL} = \frac{1}{2\pi\ 100\ 159nF} = 10KHz$$

The higher frequency poles of the unmodified PA88 Aol must be added into the modified Aol as shown in Figure 31.

STEP 2: Calculate DC ß for circuit, Cn is an open for DC.

DC ß = RI/(RF+RI) = 1K/(274K+1K) = .003636363
DC 1/ß = 20 Log (1/.03636363) = 48.79 dB

STEP 3: Plot DC 1/ß. Add noise gain compensation using the hints given above. Things look okay. We have 20 dB per decade rate of closure. fp is a decade away from fcl. High frequency 1/ß is less than 20 dB greater than low frequency 1/ß, and fz is less than a decade spaced from fp.

STEP 4: Plot open loop phase plot as in Figure 32 (see following page) from the information given in Figure 31. We see from this plot we have 45 degrees of phase margin.

5.3 COMPOSITE AMPLIFIER & STABILITY

There are design cases where the input characteristics of a power op amp may not be sufficient to meet required specifications. In these cases one can still have the advantages of using

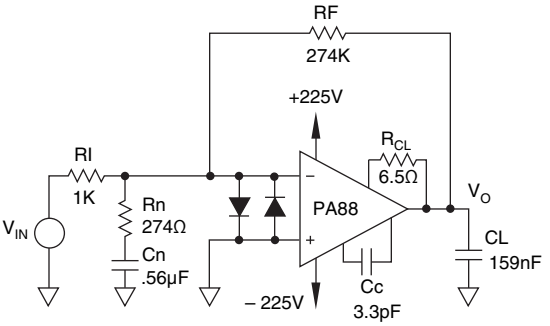


FIGURE 30. NOISE GAIN COMPENSATION FOR CL

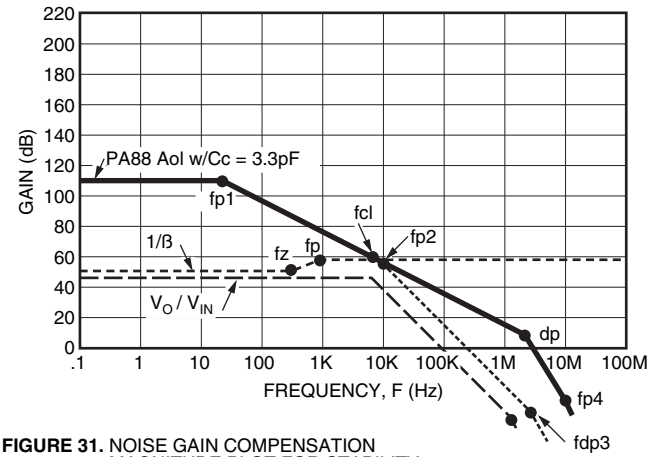


FIGURE 31. NOISE GAIN COMPENSATION MAGNITUDE PLOT FOR STABILITY

the power op amp for linear analog control, but can optimize the front end of the circuit to meet the required specifications. A composite amplifier such as Figure 33 (see following page) will provide a highly accurate 75uV input offset voltage versus the 40 mV input offset voltage of the PA241. In the composite amplifier, the PA241 acts as a booster running in a closed loop gain of 11. The PA241 "booster"" and the OP07 form a new composite amplifier with the feedback from output all the way

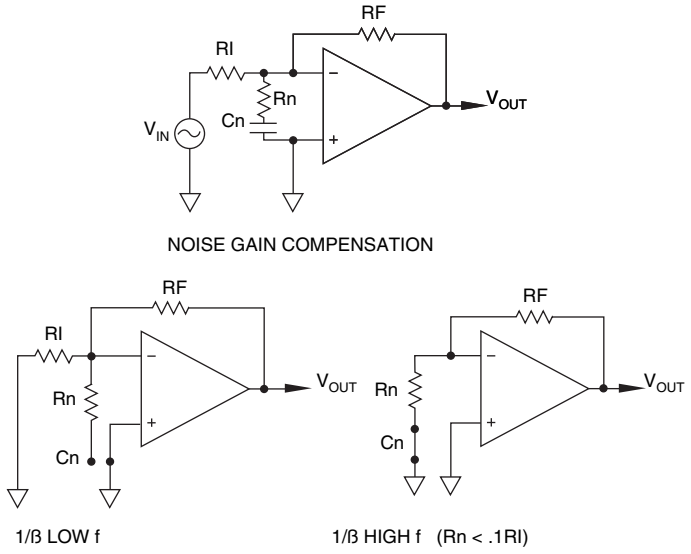
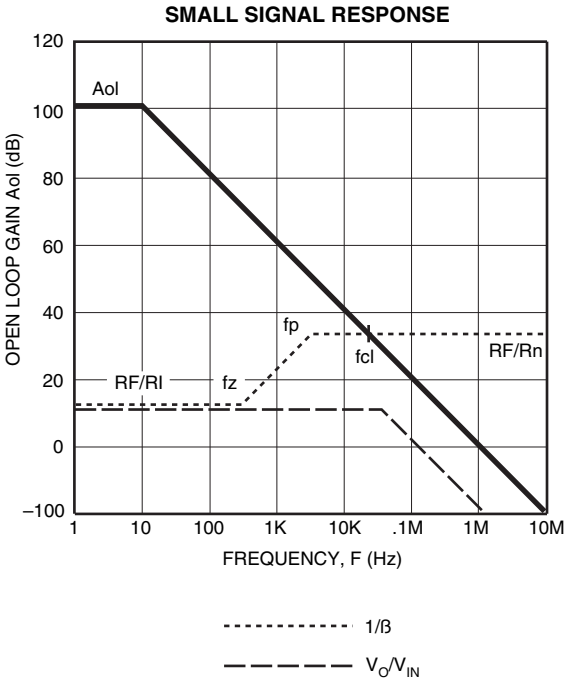


FIGURE 29. NOISE-GAIN COMPENSATION



back to the input of the OP07.

The application in Figure 33 (next page) provides an excellent opportunity for us to utilize our knowledge of stabilizing circuits with capacitive loads, as well as acquire new techniques for dealing with stability and composite amplifiers.

The following steps will provide a simple, logical approach

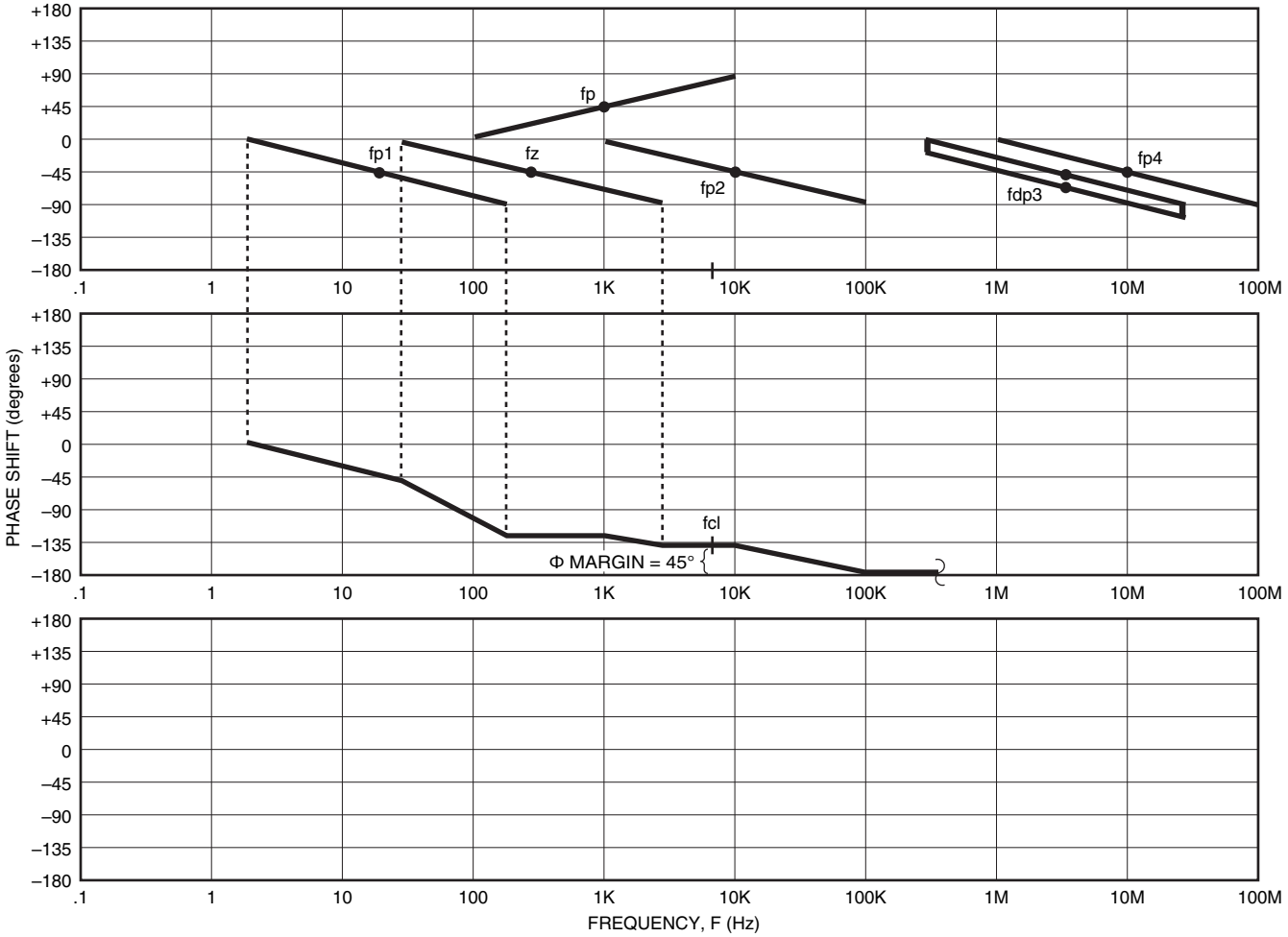


FIGURE 32. NOISE GAIN COMPENSATION OPEN LOOP PHASE PLOT FOR STABILITY

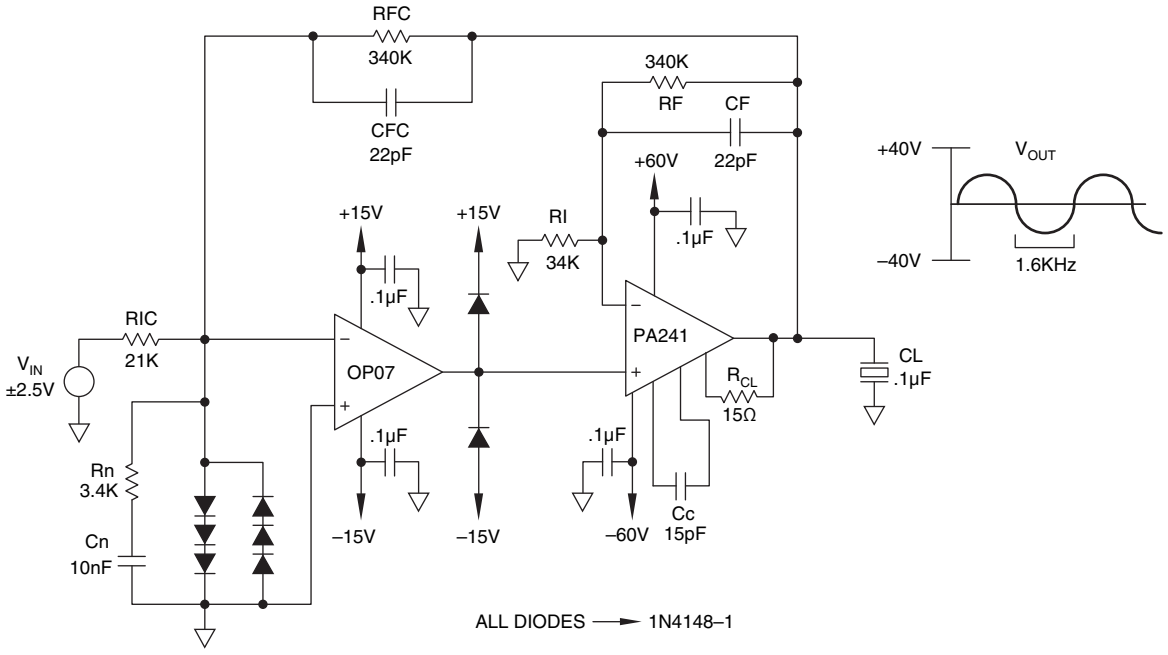


FIGURE 33. PA241 COMPOSITE PIEZO TRANSDUCER DRIVE

to attacking composite amplifier stability problems:

STEP 1: Given specifications:

V_{IN} = ± 2.5 VOLTS
DC ≤ fin ≤ 1.6 KHz
CL = .1µF
V_{OUT} = –/+ 40 VOLTS
± 15 Volts available in system
Input offset voltage ≤ 100µV

STEP 2: From given specifications determine maximum slew rate needed to track highest frequency output.

S.R. [V/µs] = 2(π)f Vopk (1x10–6)
S.R. = 2(π) (1.6K) 40V (1x10–6) = .4V/µs

STEP 3: From calculated slew rate and given CL, determine current needed to drive capacitive load.

I = C dV/dt
I = .1µF (.4V/µs) = 40mA

STEP 4: Select power op amp and host amplifier.
PA240 is the lowest cost power op amp with 40mA of output capability; a slew rate of 20V/us, with Cc=15pF, and Vsat of 12V at 40mA out. PA241 is the same monolithic chip, but in a package with enough pins for programmable current limit. In this application, fault tolerance afforded by having current limit justifies the additional cost of the PA241.

OP07 will provide 75µV of input offset voltage; a slew rate of .17 V/µs; and an output voltage swing of +/-12V from +/-15V supplies. The maximum output voltage swing of the host times the booster gain must meet the desired output voltage swing. Here there is no problem since +/-12V out of OP07 times 11 (booster gain) will yield potential for +/-120V out of the composite amplifier configuration.

The slew rate of the host amplifier times the booster gain should be less than or equal to the booster slew rate. If it is greater than the booster slew rate, the host amplifier can "outrun" the booster during high slew rate demands and consequently the composite amplifier will be running open loop and hence non-linearities and distortion will be uncontrolled.

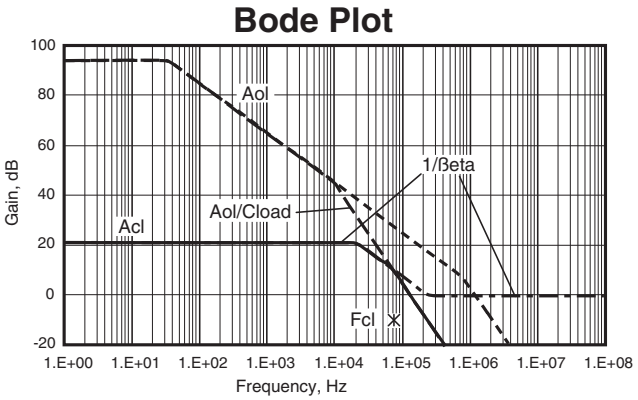
Host S.R. x Booster Gain = .17/µs x 11 = 1.87V/µs
1.87V/µs < 20V/µs (Booster S.R.)

We will run the booster amplifier in a closed loop gain of 11 as shown in Figure 33 to allow more margin to work with when compensating the capacitive load. We know this from experience in designing many power op amp circuits with capacitive loads on the output.

STEP 5: The booster stage of the composite must be stable before we consider the overall composite amplifier. Booster circuit data was entered into the Cload sheet of the Apex Power Design spreadsheet. Initial indications were an intersection rate of 40dB per decade and a phase margin of only 19°. Figure 34 shows Power Design has already added the 150Ω amplifier output impedance to the 15Ω current limit resistor and calculated the pole with the capacitive load to be at 9.6KHz. The booster stage was compensated with Cf producing a closed loop pole (a feedback zero) at 21.3KHz. Do not be confused by sub-Hertz or multi-GHz entries in the table; these show up because the spreadsheet avoids division by zero errors by forcing extremely small values for non-existent capacitors. Refer to Figure 35 to see phase contributions of all elements added, closure frequency of 75KHz, closure rate of 20dB per decade, and a phase margin of 52°.

STEP 6: We are now ready to enter the composite circuit data as shown in Figure 36 (next page). Note that the closed loop gain of the booster stage has been added to the Aol of the OP07. Closure rate is 60dB per decade and we have a guaranteed oscillator. An attempt to compensate with just CFC was made, but was not good enough. A better compensation technique will use noise gain to raise the 1/ß curve to 41.4dB and then use CFC to obtain an intersection with the composite Aol of 20dB per decade.

MODEL	PA241,3-150	Note/PBs	Rn	9999999999	Kohms
Rcl	15	Ohms	Cn	0	nF
Cload	0.1	uF	Cf	22	pF
Rin	34	Kohms	Riso	0	Ohms
Rf	340	Kohms			



Total Rout	165	Ohms
Pole Zout/Cload	9.645744481	KHz
1/Beta (DC)	20.8	dB
Noise Gain	0.0	dB
Pole Noise Gain	0.159154943	KHz
Zero Noise Gain	0.159154938	KHz
Pole Cf/Rf	21.27739784	KHz
Zero Rf/Cf	234.051377	KHz
Zero Riso/Cload	1.59155E+11	KHz

FIGURE 34.

Phase Shift Components

Estimated Closure Frequency =	74.98942	KHz
Suggested maximum bandwidth	11.54782	KHz
Estimated Closure Rate =	20.0	dB/decade
Estimated Phase Margin =	51.78278	Degrees

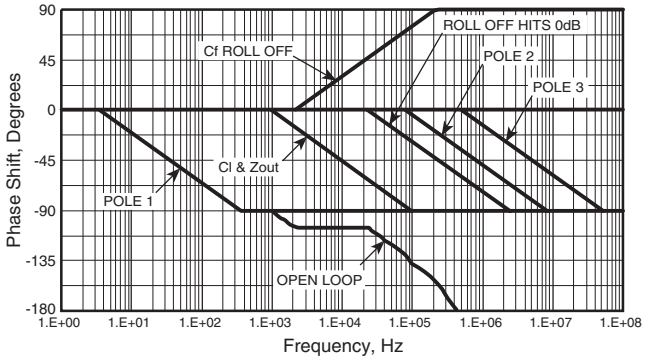


FIGURE 35.

STEP 7: Figure 37 (next page) shows the effect of adding our stabilization components. We have achieved the desired intersection rate of 20dB per decade. Note that the output signal does not rise at 686Hz when the noise gain kicks in, but does begin to roll off at 21.3KHz due to the 22pF roll off capacitor.

Once again our final stability check is completed by the open loop phase plot for the composite amplifier as shown in Figure 38 (next page). The resultant 50 degrees of phase margin

guarantees a stable composite amplifier configuration.

P.S. — Refer to Figure 33. The 1N4148-1 diodes on the input of the OP07 provide differential and common mode overvoltage protection from transients through CFC. Piezo elements being electromechanical devices can generate high voltages if shocked mechanically. Output diodes of the OP07 prevent overvoltage transients that occur through CF and shunted through PA241 internal input protection diodes, from damaging the output of the OP07 connected to +input of PA241.

MODEL	OP07	READ ME			
Aol =	135	dB	Pole 1 =	0.1	Hz
Pole 2 =	7.00E+05	Hz	Pole 3 =	7.00E+06	Hz
Rin	21	Kohms	Rn	999999999	Kohms
Rf	340	Kohms	Cn	0	nF
Cf	0	pF	Using Look-Up data		

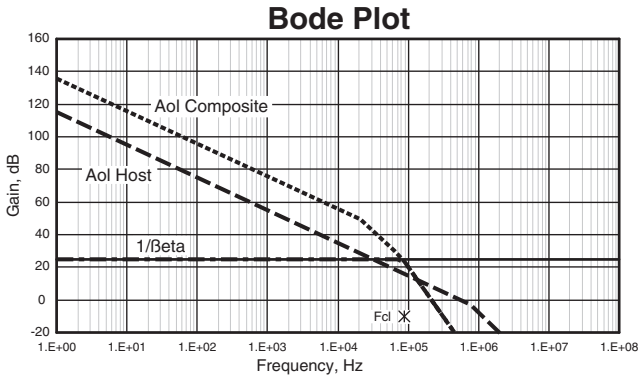


FIGURE 36.

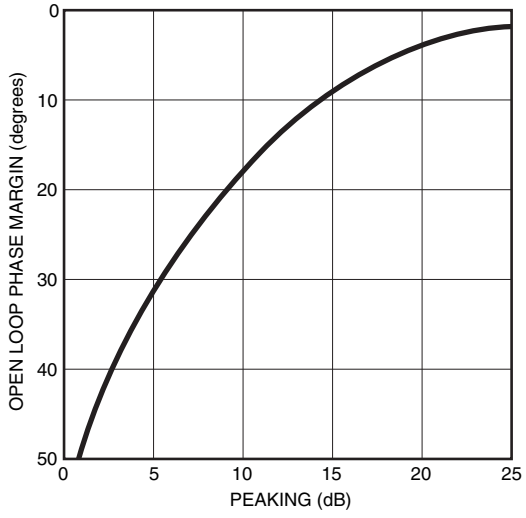
6.0 REAL WORLD STABILITY TESTS

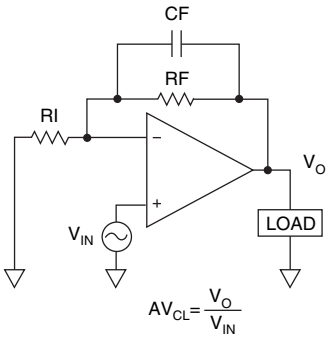
We have devoted much text to discussing how to design stable circuits. Once a circuit is designed and built it is often difficult to open the feedback path in the real world and measure open loop phase margin for stability.

The following Real World Stability Tests offer methods to verify if predicted open loop phase margins actually make it to the real world implementation of the design. Although the curves shown for these tests are only exact for a second order system, they provide a good source of data since most power op amp circuits possess a dominant pair of poles that will be the controlling factor in system response.

6.1 AVCL PEAKING TEST

Figure 39 illustrates the AVcl Peaking Test for measuring open loop phase margin in the real world closed loop domain.





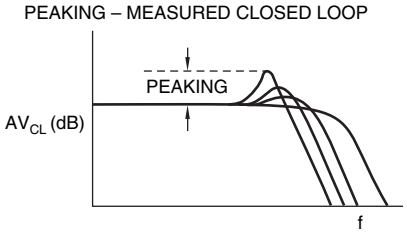
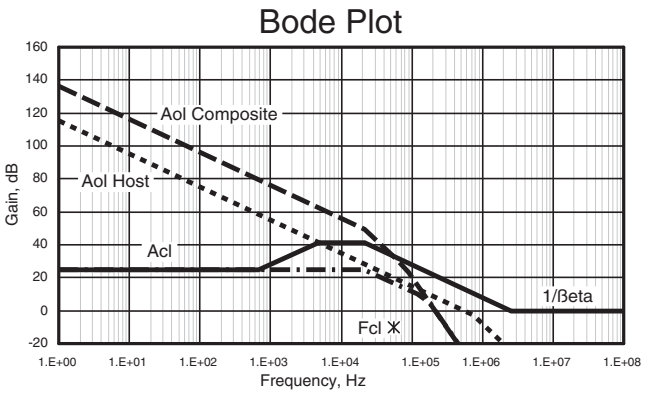


FIGURE 39. AV_{CL} PEAKING TEST

MODEL	OP07	READ ME			
Aol =	135	dB	Pole 1 =	0.1	Hz
Pole 2 =	7.00E+05	Hz	Pole 3 =	7.00E+06	Hz
Rin	21	Kohms	Rn	3.4	Kohms
Rf	340	Kohms	Cn	10	nF
Cf	22	pF	Using Look-Up data		



1/Beta (DC)	24.7	dB
Noise Gain	16.7	dB
Pole Noise Gain	4.681027677	KHz
Zero Noise Gain	0.68665214	KHz
Pole Cf/Rf	21.27739871	KHz
Zero Rf/Cf	2493.508487	KHz

FIGURE 37.

Estimated Closure Frequency =	56.23413	KHz
Suggested maximum bandwidth	5.623413	KHz
Estimated Closure Rate =	20.0	dB/decade
Estimated Phase Margin =	50.625	Degrees

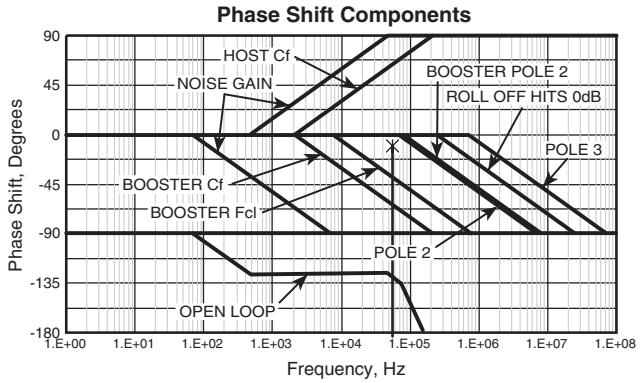


FIGURE 38:

From the closed loop Bode plot, we can measure the peaking in the region of gain roll-off. This will directly correlate to open loop phase margin as shown.

6.2 SQUARE WAVE TEST

Figure 40 illustrates the Square Wave Test for measuring open loop phase margin by closed loop tests. The output amplitude of the square wave is adjusted to be 2 Vpp at a frequency of 1 kHz. The key elements of this test are to use low amplitude (AC small signal) and a frequency that will allow ease of reading when triggered on an oscilloscope. Amplitude adjustment on the oscilloscope wants to accentuate the top of the square wave to measure easily the overshoot and ringing. The results of the test can be compared to the graph in Figure 40 to yield open loop phase margin.

A complete use of this test is to run the output symmetrical about zero with +/-1V peak and then re-run the test with various DC offsets on the output above and below zero. This will check stability at several operating points to ensure no anomalies show up in field use.

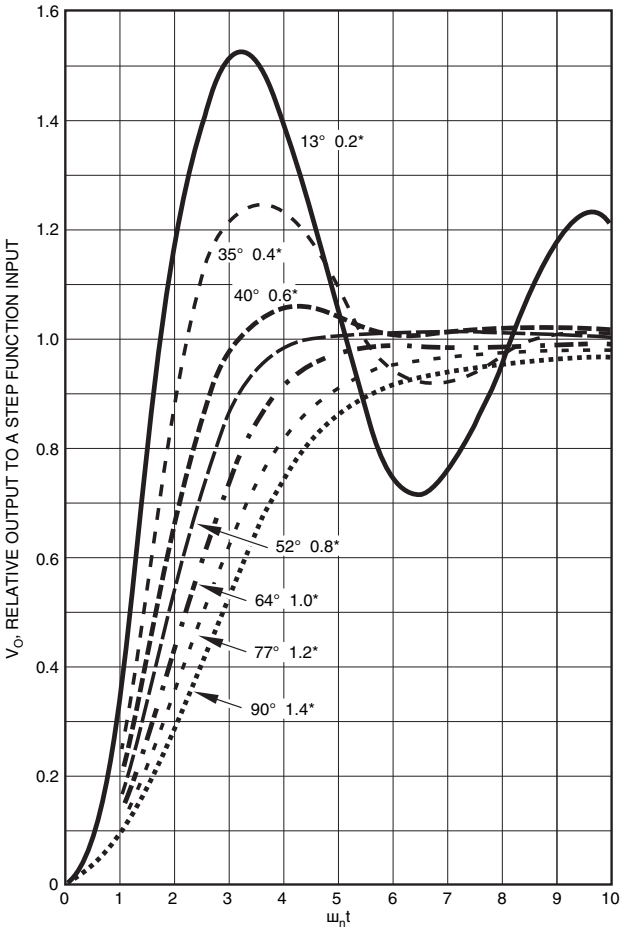


FIGURE 40. SQUARE WAVE TEST

6.3 DYNAMIC STABILITY TEST

An expansion on the Square Wave Test is shown in Figure 41(see second page following this one). The Dynamic Stability Test superimposes a small signal AC square wave on a low frequency, large signal AC sinewave to dynamically test the power op amp circuit under all operating point conditions. The resultant ringing on the square wave can be compared to the graph in Figure 40 for relation to open loop phase margin. Note that R1 // R2 in Figure 41 must be much greater than RIN or the input summing test impedances will affect the compensation of the power op amp circuit under test.

7.0 STABILITY TROUBLESHOOTING GUIDE

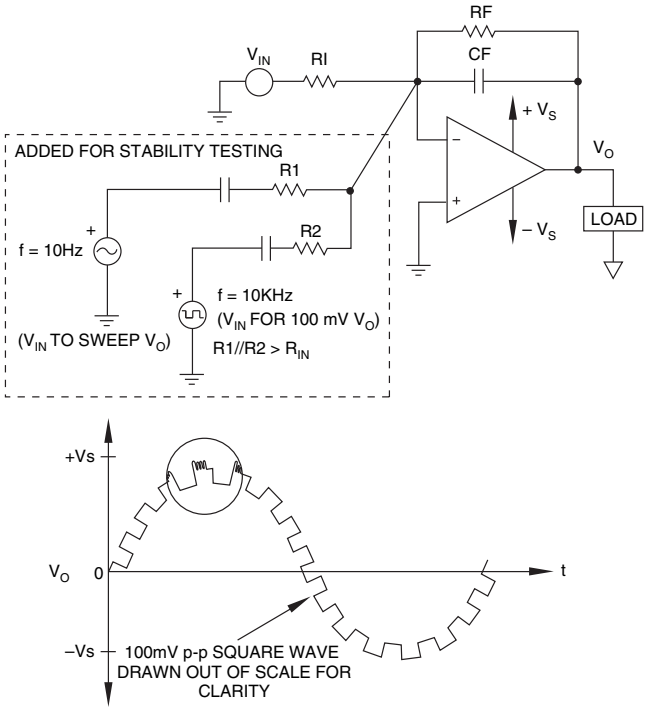


FIGURE 41. DYNAMIC STABILITY TEST

Figure 42 (see third page following this one) provides a troubleshooting guide for the most common stability problems. The “Probable Cause/Possible Solution Key” gives insight into the origin of the problem and provides guidance as to the appropriate fix.

8.0 FINAL STABILITY NOTE

When you’re at your wits end trying to solve an oscillation problem, don’t give up because you have it down to an “acceptably low” level. A circuit either oscillates or it doesn’t, and no amount of oscillation is acceptable. Apply the techniques and ideas in this Application Note under your worst case load conditions and you can conquer your oscillation problems.

If time is short or you can’t see the forest from the trees, APEX would be happy to provide Technical Support via FAX, 602-888-7003, or via the Applications Hotline, 800-546-2739 (USA & CANADA, outside Arizona only). Or call direct, 520-690-8600. More importantly, as we tell all our customers, we would be happy to review your schematic for stability considerations, etc., before you ever build a circuit or even buy a power op amp.

9.0 REFERENCES

1) Frederiksen, Thomas M. : INTUITIVE IC OP AMPS, R.R. Donnelley & Sons, 1984.
2) Huelsman, Lawrence P. : BASIC CIRCUIT THEORY WITH DIGITAL COMPUTATIONS, Prentice-Hall, Inc., Englewood Cliffs, N.J., 1972.
3) Faulkenberry, Luces M. : AN INTRODUCTION TO OPERATIONAL AMPLIFIERS WITH LINEAR IC APPLICATIONS, John Wiley & Sons, New York, 1982.
4) Dorf, Richard C. : MODERN CONTROL SYSTEMS (Third Edition), Addison-Wesley Publishing Company, Reading, Massachusetts, 1980.

CONDITION AND PROBABLE CAUSE TABLE

Oscillation Frequency	Oscillates unloaded?	Oscillates with V_{IN} = 0?	Loop Check† fixes oscillation?	Probable Cause(s) (in order of probability)
$f_{osc} \leq$ UGBW	N	Y	N	C, D
$f_{osc} \leq$ CLBW	Y	Y	Y	K, E, F, J
$f_{osc} \leq$ UGBW	–	–	N	G, A, M, B
$f_{osc} \leq$ CLBW	N	Y	Y	D
$f_{osc} \leq$ UGBW	Y	Y	N*	J, C
$f_{osc} \leq$ CLBW	Y	Y	N	L, C
$f_{osc} >$ UGBW	N	Y	N	B, A
$f_{osc} >$ UGBW	N	N**	N	A, B, I, H

CLBW = Closed Loop Bandwidth
UGBW = Unity Gain Bandwidth
† See Figure 42A for loop check circuit.
— Indeterminate; may or may not make a difference.
*Loop check (Figure 42A) will stop oscillation if Rn << $|X_{CF}|$ at UGBW.
**Only oscillates over a portion of the output cycle.

KEY TO PROBABLE CAUSE / POSSIBLE SOLUTION

A. Cause: Supply feedback loop (insufficient supply bypassing).
Solution: Bypass power supplies. See Section 2.3.
B. Cause: Supply lead inductance.
Solution: Bypass power supplies. See Section 2.3.
C. Cause: Ground loops.
Solution: Use "Star" grounding. See Figure 9.
D. Cause: Capacitive load reacting with output impedance (Aol pole).
Solution: Raise gain or use Noise Gain Compensation network. See section 5.2.4.2.
E. Cause: Inductor within the feedback loop (loop gain pole)
Solution: Use alternate feedback path. See section 5.1.
F. Cause: Input capacitance reacting with high RF (noise gain zero).
Solution: Use CF in parallel with RF. (CF =~Cin). Do not use too much CF, or you may get problem J.
G. Cause: Output to input coupling.
Solution: Run output traces away from input traces, ground the case, bypass or eliminate +RB (the bias current compensation resistor from +IN to ground)
H. Cause: Emitter follower output reacting with capacitive load.
Solution: Use output "snubber" network. See Section 2.5.
I. Cause: "Composite PNP" output stage with reactive load.
Solution: Use output "snubber network. See Section 2.5.
J. Cause: Feedback capacitance around amplifier that is not unity gain stable (integrator instability).
Solution: Reduce CF and/or increase Cc for unity gain stability.
K. Cause: Insufficient compensation capacitance for closed loop gain used.
Solution: Increase Cc or increase gain and/or use Noise Gain Compensation network. See section 5.2.4.2.
L. Cause: Servo loop stability problem
Solution: Compensate the "front end" or "servo amplifier.
M. Cause: Unwanted signals coupling into op amp through case.
Solution: Ground the case.

FIGURE 42. STABILITY TROUBLESHOOTING GUIDE

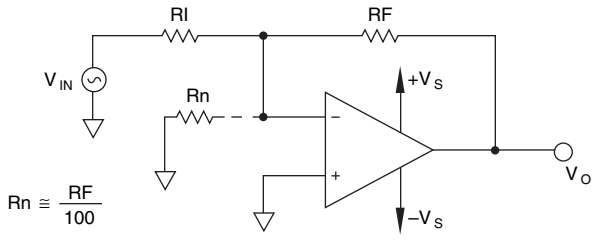


FIGURE 42A. LOOP CHECK CIRCUIT

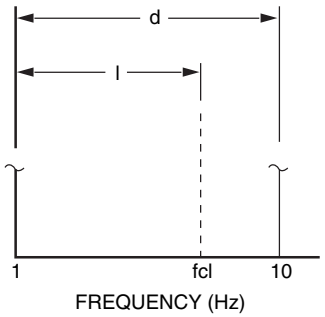
10.0 APPENDIX

This appendix contains some handy tools for plotting magnitude and phase plots for stability analyses. The "Log Scaling Technique" covers an easy way to read exact frequency locations of poles and zeroes from magnitude plots for stability. Included, as well, are blank magnitude and phase plots for copying and using to plot phase and magnitude plots for stability.

One final tip. Once a magnitude plot has been plotted containing the Aol curve and 1/ß, it is easy to translate the poles and zeroes to an open loop phase plot for stability. Simply use a light table (ours is very basic — a piece of plexiglass that fits over a 60W incandescent desk light !) to trace the locations of poles and zeroes. Remember poles and zeroes in the Aol curve are poles and zeroes in the open loop phase check for stability. But poles in the 1/ß plot become zeroes, and zeroes in the 1/ß plot become poles in the open loop phase check for stability.

LOG SCALING TECHNIQUE

When using rate-of-closure graphical techniques it is convenient to measure what frequency fp or fz might be at without detailed calculation. This handy reminder about log scale will give you that power:



$\frac{l}{d} = \text{LOG (fcl)}$

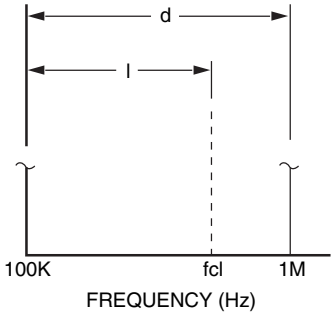
$\text{fcl} = \text{LOG}^{-1}\left(\frac{l}{d}\right)$

*$\text{fcl} = 10^{(l/d)}$

$\text{fcl} = 10^{(1.4"/2")} = 5.012\text{Hz}$

* This can be used between any decade of frequencies by normalization of scale for 1 to 10.

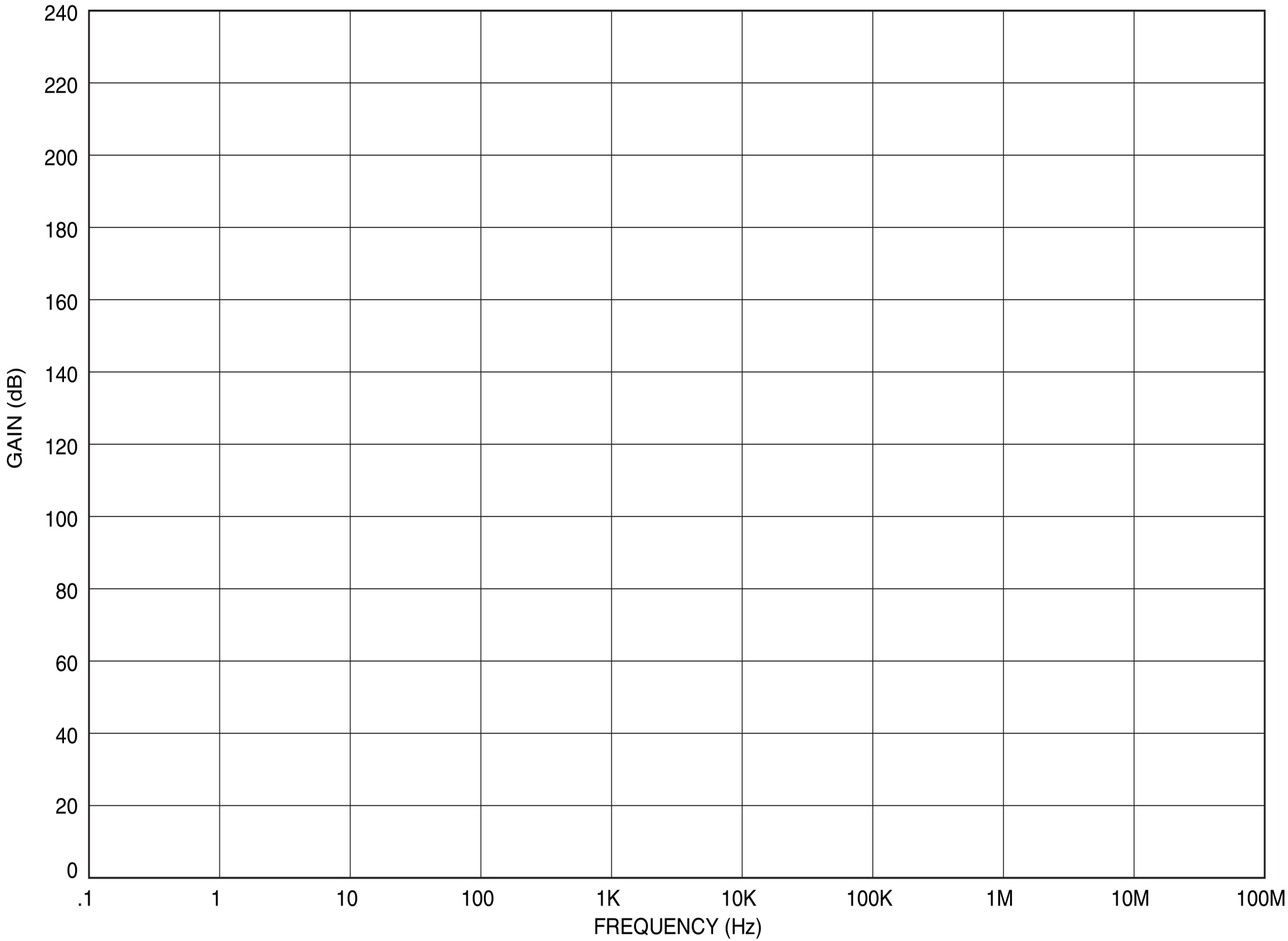
Definition by example is easiest →
What frequency is fcl below?



$\text{fcl} = 10^{(1.4"/2")} = 5.012\text{Hz}$

$\text{fcl} = 501.2\ \text{KHz}$

Scale is normalized for 1 to 10 by dividing by 100. Answer to fcl is multiplied by 100 to yield final answer in KHz.


240
220
200
180
160
140
120
100
80
60
40
20
0
GAIN (dB)
.1
1
10
100
1K
10K
100K
1M
10M
100M
FREQUENCY (Hz)